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FAIRCHILD SEMICONDUCTOR®

October 2012

FXL6408
Fully Configurable 8-Bit I²C-Controlled GPIO Expander

Features

- 4X Expansion of Connected Processor I/O Ports
- Fully Integrated I²C Slave
- 8 Independently Configurable I/O Ports
- Low-Power Quiescent Current: 1.5 µA
- Voltage Translation Capable from 1.65 V I²C Port Up to 4.0 V GPIO Pins
- Selectable Device Address
- 6 mA Output Drive
- Interrupt Pin to Alert Processor of Status Changes

Description

The FXL6408 is an 8-bit I²C-controlled GPIO expander. When configured in Input Mode, the FXL6408 monitors the input ports for data transitions and signals the baseband by asserting the /INT pin. The input default values can be programmed independently, allowing customized input detection. All inputs can be configured with pull-up or pull-down resistors to pre-bias the inputs in open-drain or non-driven applications. When configured in Output Mode, the GPIO pins are capable of delivering 6 mA output drive according to the I²C register set. The FXL6408 is designed to allow voltage translation from levels as low as 1.65 V and up to 4.0 V. The FXL6408 features an active LOW RESET input as well as Power-On Reset (POR) circuit and I²C software reset options.

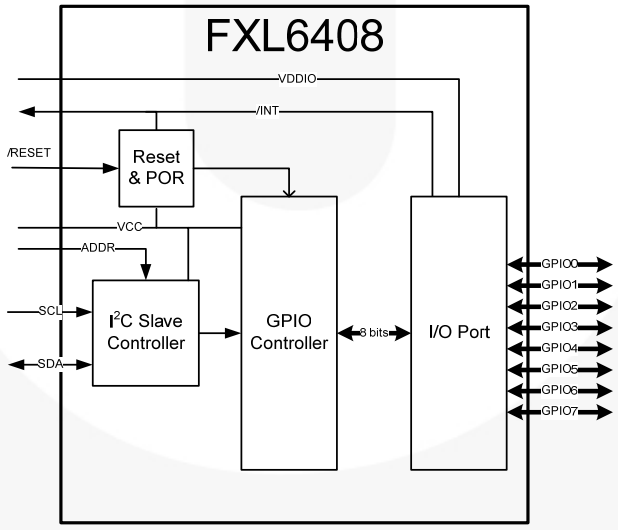


Figure 1. Block Diagram

Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package	Packing Method
FXL6408UMX	XT	-40 to 85°C	16-Lead, UMLP, Quad, Ultrathin MLP, 1.8 X 2.6 mm Body	5000 Units on Tape and Reel

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Pin Configurations

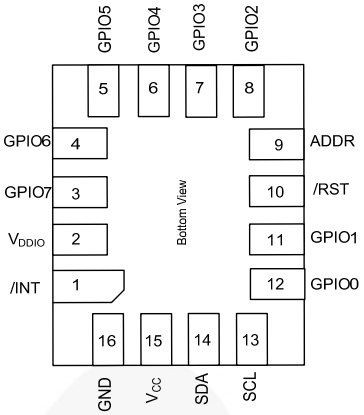


Figure 2. Bottom View

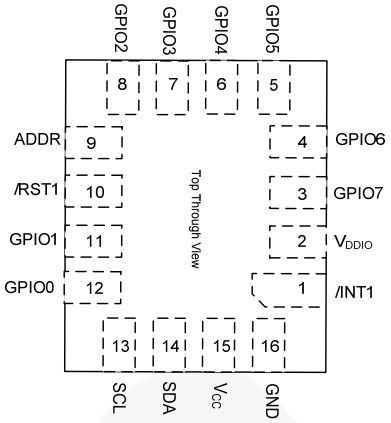


Figure 3. Top Through View

Pin Descriptions

Pin #	Pin Name	Description
1	/INT	Interrupt output, open-drain, active LOW; requires an external pull-up resistor to V_{CC}
2	V_{DDIO}	Voltage reference for I/O-side voltage translation (if I/O translation is not needed, tie V_{DDIO} to the V_{CC} supply)
3	GPIO7	General-purpose programmable I/O
4	GPIO6	General-purpose programmable I/O
5	GPIO5	General-purpose programmable I/O
6	GPIO4	General-purpose programmable I/O
7	GPIO3	General-purpose programmable I/O
8	GPIO2	General-purpose programmable I/O
9	ADDR	Address input, GND or V_{CC}
10	/RST	Reset input, active LOW, requires a pull-up resistor to V_{CC}
11	GPIO1	General-purpose programmable I/O
12	GPIO0	General-purpose programmable I/O
13	SCL	I^2C serial bus; requires a pull-up resistor to V_{CC}
14	SDA	I^2C serial data; requires a pull-up resistor to V_{CC}
15	V_{CC}	Supply voltage
16	GND	Ground

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{CC}, V_{DDIO}	Supply Voltages		-0.5	4.6	V
V_{IN}	DC Input Voltage		-0.5	4.0	V
V_{OUT}	Output Voltage[1]		-0.5	4.0	V
I_{IK}	DC Input Diode Current	V_{IN} < 0 V		-50	mA
I_{OK}	DC Output Diode Current	V_{OUT} < 0 V		-50	mA
I_{OL}	DC Output Sink Current			+50	mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin			±100	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature under Bias			+150	°C
T_L	Junction Lead Temperature, Soldering 10 Seconds			+260	°C
Θ_{JA}	Thermal Resistance, Junction-to-Ambient			115	°C/W
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4	kV
		Charged Device Model, JESD22-C101		2	

Note:
1. All output current absolute maximum ratings must be observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Condition	Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	3.60	V
V_{DDIO}	I/O Side Reference Voltage		1.65	4.00	V
V_{IN}	Input Voltage on I/O pins		0	4.0	V
V_{OUT}	Output Voltage		0	V_{DDIO}	V
T_A	Operating Temperature		-40	+85	°C
t_r, t_f	Input Rise and Fall Times to I/O Pins when Configured as Inputs	V_{DDIO} at 1.8 V, 2.5 V ±0.2 V	0	200	ns/V
		V_{DDIO} at 3.6 V ± 0.3 V	0	100	

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DC Electrical Characteristics

Symbol	Parameter	Condition	V_{CC} (V)	T_A=25°C			T_A=-40 to 85°C		Unit
				Min.	Typ.	Max.	Min.	Max.	
RST, ADDR, SDA, SCL, /INT Pins									
V_{POR}	Power-On Reset Voltage	V_{DDIO}=0 to 4.0 V				1.25		1.25	V
I_{IN}	Input Leakage Current	$0 \le V_{IN} \le V_{CC}$	0 to 3.6			±1		±10	µA
I_{OFF}	Power-Off Leakage Current	V_{IN} or V_{OUT}=3.6 V	0			1		10	µA
I_{CC}	Standby Mode (SCL in Static Condition)	$V_{IN}=V_{CC}$ or GND	1.8 to 3.6			1.2		1.5	µA
	Active Mode[2] (SCL Active)					300		300	
GPIO Pins			**V_{DDIO} (V)**						
V_{IH}	HIGH Level Input Voltage		1.65 to 1.95	0.65 V_{DDIO}			0.65 V_{DDIO}		V
			2.30 to 4.00	0.70 V_{DDIO}			0.70 V_{DDIO}		
V_{IL}	LOW Level Input Voltage		1.65 to 1.95	-0.3		0.35 V_{DDIO}	-0.3	0.35 V_{DDIO}	V
			2.30 to 4.0	-0.3		0.30 V_{DDIO}	-0.3	0.30 V_{DDIO}	
V_{OH}	HIGH Level Output Voltage	$V_{IN}=V_{IH}$, I_{OH}=100 µA	1.8	V_{DDIO} - 0.2			V_{DDIO} - 0.2		V
			3.6	V_{DDIO} - 0.2			V_{DDIO} - 0.2		
			4.0	V_{DDIO} - 0.2			V_{DDIO} - 0.2		
		I_{OH}=6 mA	1.8	V_{DDIO} - 0.45			V_{DDIO} - 0.45		
			3.6	V_{DDIO} - 0.45			V_{DDIO} - 0.45		
V_{OL}	LOW Level Output Voltage	$V_{IN}=V_{IL}$, I_{OL}= -100 µA	1.8			0.2		0.2	V
			3.6			0.2		0.2	
			4.0			0.2		0.2	
		I_{OL}=-6 mA	1.8			0.45		0.45	
			3.6			0.5		0.5	
R_{PULL}	Pull-Up or Pull-Down Resistors				100				kΩ
I_{OL}	Output Low Current		1.8 to 4.0	6.0			6.0		mA
I_{OH}	Output High Current		1.8 to 4.0	-6.0			-6.0		
I_{IN}	Input Low Current[3]	$0 \le V_{IN} \le V_{DDIO}$	1.8 to 4.0			±50		±50	µA
I_{OFF}	Power-Off Leakage Current	V_{IN}=4.0 V	0			1		10	µA

Notes:

2. Includes all internal circuitry consumption from the V_{CC} supply. Does not include the I/O buffers, which are supplied by V_{DDIO} and are load dependent.
3. I_{IL} and I_{IH} specifications only apply when the outputs are configured with pull-down or pull-up resistors, respectively. Specifications values assume V_{IN} <= V_{DDIO}.

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AC Electrical Characteristics

All typical value are for V_{CC}=1.8 V at T_A = 25°C unless otherwise specified.

Symbol	Parameter	Fast Mode		
		Min.	Max.	Unit
t_w	Reset Pulse Duration (*see Figure 4*)	150		ns
t_{RST_GLITCH}	Input Glitch Rejection on RST Pin (*see Figure 4*)	50	150	ns
t_{RESET}	Reset Time, Total Time from Rising Edge of Reset Pulse to Falling Edge of /INT Pin (*see Figure 5*)		150	ns
t_{IV}	Time from Input Default State Change to /INT Pin Driven LOW (*see Figure 6*)		4	µs

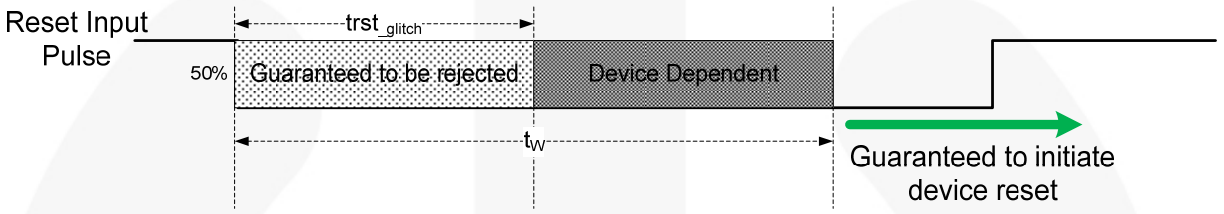


Figure 4. Reset Pulse Duration and Input Glitch Rejection Timing Diagram

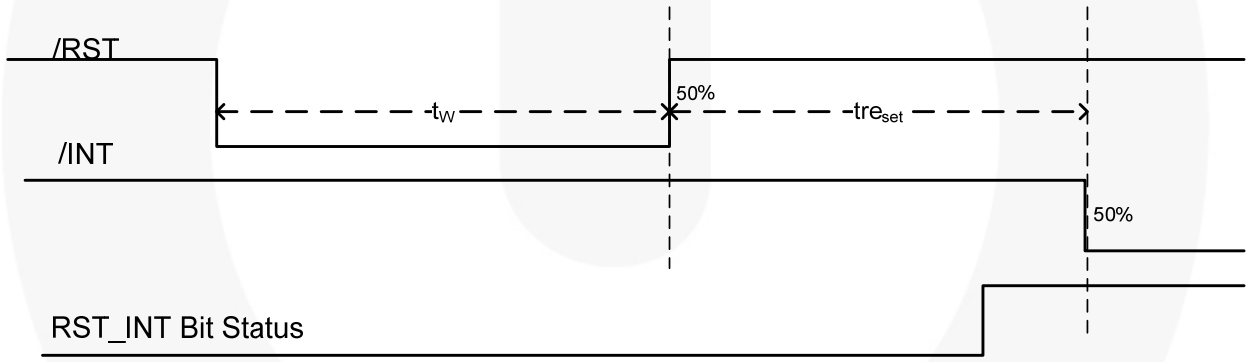


Figure 5. Reset Time and Reset Pulse Timing Diagram

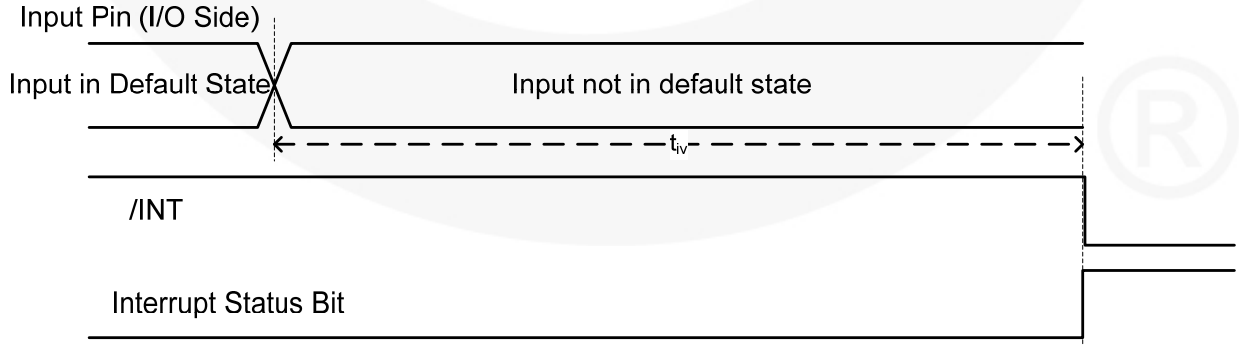


Figure 6. Time to INT from Change in Input Default State

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DC Characteristics (I²C Controller SDA, SCL)

Symbol	Parameter		Fast Mode (400 kHz)		
			Min.	Max.	Unit
V_{IL}	Low-Level Input Voltage		-0.5	0.3 V_{CC}	V
V_{IH}	High-Level Input Voltage		0.7 V_{CC}		V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	V_{CC} > 2 V	0.05 V_{CC}		V
		V_{CC} < 2 V	0.1 V_{CC}		
V_{OL}	Low-level Output Voltage at 3 mA Sink Current (Open-Drain or Open-Collector)	V_{CC} > 2 V	0	0.4	V
		V_{CC} < 2 V		0.2 V_{CC}	V
I_I	Input Current of Each I/O Pin, Input Voltage 0.26 V to 2.34 V		-10	10	µA
C_I	Capacitance for Each I/O Pin			10	pF

AC Electrical Characteristics (I²C Controller SDA, SCL)

All typical value are for V_{CC}=1.8 V at T_A=25°C unless otherwise specified.

Symbol	Parameter	Fast Mode (400 kHz)		
		Min.	Max.	Unit
f_{SCL}	SCL Clock Frequency	0	400	kHz
$t_{HD;STA}$	Hold Time (Repeated) START Condition	0.6		µs
t_{LOW}	LOW Period of SCL Clock	1.3(4)		µs
t_{HIGH}	HIGH Period of SCL Clock	0.6		µs
$t_{SU;STA}$	Set Up Time for Repeated START Condition	0.6		µs
$t_{HD;DAT}$	Data Hold Time (*See Figure 7*)	0	0.9	µs
$t_{SU;DAT}$	Data Set Up Time (*See Figure 7*)	100(5)		ns
t_{PS}	Set Up Time Required by SDA Input Buffer (When Receiving Data)	0		ns
t_{PH}	Out Delay Required by SDA Output Buffer (When Transmitting Data)	300		ns
t_r	Rise Time of SDA and SCL Signals	20+0.1C_b(6,7)	300	ns
t_f	Fall Time of SDA and SCL Signals	20+0.1C_b(6,7)	300	ns
$t_{SU;STOP}$	Set Up Time for STOP Condition	0.6		µs
t_{BUF}	Bus Free Time between a STOP and START Conditions	1.3		µs
t_{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

4. The FXL6408 can accept clock signals with LOW as low as 1.1 µs, provided that the received SDA signal $t_{HD;DAT}$+ $t_{r/f}$<=1.1 µs. The FXL6408 features a 0 ns SDA input setup time and, therefore, this parameter is not included in the above equation.
5. A Fast-Mode I²C-Bus® device can be used in a Standard-Mode I²C-Bus system, but the requirement $t_{SU;DAT}$ ≥ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal. It must output the next data bit to the SDA line t_{r_max} + $t_{SU;DAT}$ = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C bus specification) before the SCL line is released.
6. C_b equals the total capacitance of one bus line in pF. If mixed with High-Speed Mode devices, faster fall times are allowed, according to the I²C specification.
7. The FXL6408 ensures that the SDA signal out must coincide with SCL LOW for worst-case SCL t_f maximum times of 300 ns. This requirement prevents data loss by preventing SDA out transitions during the undefined region of the falling edge of SCL. Consequently, the FXL6408 fulfils the following requirement from the I²C specification, note 2 on page 77: "A device must internally provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL."
8. FXL6408 I²C slave is fully compliant the NXP (Phillips) I²C specification Rev. 0.3 UM10204 (2007).

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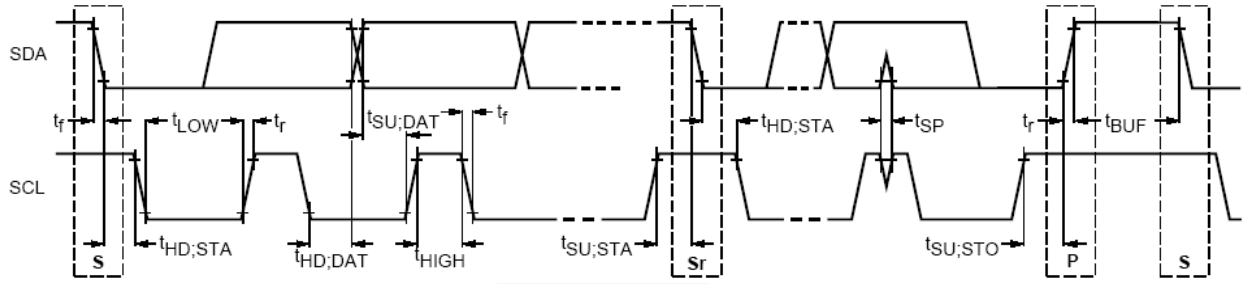


Figure 7. Definition of Timing for Full-Speed Mode Devices on the I²C-Bus®

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Functional Description

Overview

The FXL6408 I/O expander frees up six ports of the central processor to be dedicated for more critical functions. The FXL6408 enables the addition of eight General-Purpose Input / Output (GPIO) ports to a system processor while using two I/O ports for I^2C control (net six additional I/Os). The device can be used in multiple applications, from button monitoring to driving control pins of other ICs in the system. It also allows the system designer to add new features and functions quickly without upgrading the central processor. The FXL6408 includes eight I/O pins controlled by an integrated I^2C slave and allows the central processor to control each I/O independently. When configured as outputs, each pin can deliver up to 6 mA drive. When configured as inputs, the default state can be independently configured. In addition, the FXL6408 has integrated pull-up and pull-down resistors that are enabled via I^2C commands in the register map. This allows the system designer to pre-bias the inputs to a known level to allow use with un-driven input signals.

Interrupt Operation

The /INT pin is a LOW-asserted open-drain output and requires an external pull-up resistor. The FXL6408 signals an interrupt to the processor when an event occurs, removing the need for the processor to continuously poll the FXL6408 registers. Immediately after detecting a change at an input, the FXL6408 writes the corresponding bit in the input interrupt status register (13_h) and asserts the /INT pin by pulling it LOW. The interrupt status register bit remains HIGH until the processor reads the register and clears the bit. If the input pin remains in the non-default state after the interrupt has been serviced, a new interrupt is not generated until after the input state has first returned to its default state and changed back to its non-default state. The FXL6408 also contains an Input Status register ($0F_h$) used to verify the current status of the given input at the time when the interrupt is serviced by the processor. These two registers allow the processor to determine the following information about any input every time the register map is read:

- If the input state changed from the default state since the most recent register read; and
- The current state of the input pin.

The interrupt output /INT, once asserted, is held LOW until the interrupt is serviced by the processor. This means that the system uses level-sensitive interrupts. Interrupt signaling is asynchronous to the SCL signal.

Device Reset

The FXL6408 has three reset options, all of which cause the part to reset all register settings to their default states. Immediately after device reset, the RST_INT bit in the Device ID & Ctrl register (01h) is HIGH and an interrupt signal is generated by the FXL6408. After the processor reads the register, this bit is cleared and, on future register reads, the processor can verify that the FXL6408 has not been reset if this bit remains LOW. Following are descriptions of the three reset methods.

Power-On Reset (POR)

On device power-up, when V_{CC} reaches V_{POR} or if the V_{CC} supply voltage drops below V_{POR} during operation, the FXL6408 immediately resets.

Software Reset

The FXL6408 can be reset by the processor using an I^2C write command to change bit 0 of register 01h to a 1. Immediately following this change, the FXL6408 resets and all register values return to their default values. In this case, the SW_RST bit returns to 0 as soon as the reset sequence is completed.

Reset Pin

The FXL6408 is reset when the /RST pin (C3) is pulled LOW.

Translation

The FXL6408 has the ability to translate between the system I^2C voltage reference and the I/O voltage reference. The V_{CC} pin is used both as the FXL6408 power supply as well as the voltage reference for the I^2C inputs, ADDR, /INT, and RESET pins. The V_{DDIO} pin is used only for the voltage supply reference of the I/O ports. For example, a 1.8 V-referenced I^2C Bus can be used to interface with the FXL6408 and control 3.6 V-referenced I/Os by supplying V_{CC} = 1.8 V and V_{DDIO} = 3.6 V. If translation is not needed, the system provides the same voltage to both the V_{CC} and V_{DDIO} pins. If both the I/O and I^2C interfaces are referenced to 1.8 V, the V_{CC} supply and V_{DDIO} pin should both be tied to 1.8 V.

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I²C Read / Write Procedures

Figure 8 and Figure 9 illustrate compatible I²C write and read sequences. The FXL6408 does not support burst read or write optional modes described in the I²C standard.

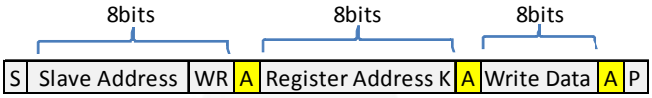
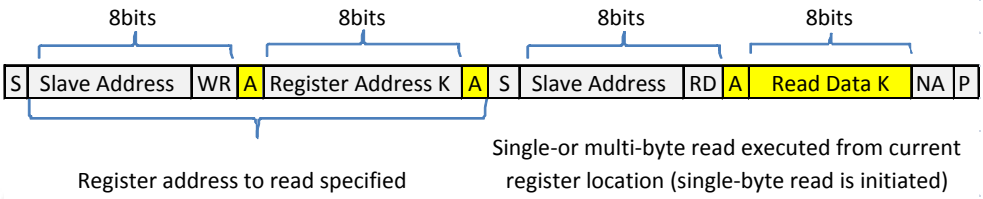


Figure 8. I²C Write Sequence



Note: If register is not specified, the master reads from the current register.

Figure 9. I²C Read Sequence

From Master to Slave
From Slave to Master

S Start Condition
A Acknowledge (SDA Low)
NA NOT Acknowledge (SDA High)
WR Write=0
RD Read =1
P Stop Condition

Table 1. I²C Address

Register	ADDR Pin	B7	B6	B5	B4	B3	B2	B1	B0
Device Address	ADDR=0	1	0	0	0	0	1	1	WR
	ADDR=1	1	0	0	0	1	0	0	WR

Table 2. I²C Register Map

Register	Address	Type	B7	B6	B5	B4	B3	B2	B1	B0	Reset Value
Device ID & Ctrl	01h	R/W	MF3	MF2	MF1	FW_rev3	FW_rev2	FW_rev1	RST_INT	SW_RST	10100010
IO Direction	03h	R/W	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	00000000
Output State	05h	R/W	Out 7	Out 6	Out 5	Out 4	Out 3	Out 2	Out 1	Out 0	00000000
Output High-Z	07h	R/W	Out 7	Out 6	Out 5	Out 4	Out 3	Out 2	Out 1	Out 0	11111111
Input Default State	09h	R/W	In 7	In 6	In 5	In 4	In 3	In 2	In 1	In 0	00000000
Pull Enable	0Bh	R/W	In 7	In 6	In 5	In 4	In 3	In 2	In 1	In 0	11111111
Pull-Down/ Pull-Up	0Dh	R/W	In 7	In 6	In 5	In 4	In 3	In 2	In 1	In 0	00000000
Input Status	0Fh	R	In 7	In 6	In 5	In 4	In 3	In 2	In 1	In 0	XXXXXXXX
Interrupt Mask	11h	R/W	In 7	In 6	In 5	In 4	In 3	In 2	In 1	In 0	00000000
Interrupt Status	13h	R/W	In 7	In 6	In 5	In 4	In 3	In 2	In 1	In 0	XXXXXXXX
Reserved	02h, 04h, 06h, 08h, 0Ah, 0Ch, OEh,10h, 12h	Reserved	XXXXXXXX								

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Table 3. Device ID & Control

- Address 01_h
- RST INT flag is cleared after being read by master.
- For SW reset, the master writes bit 0 HIGH.

Bit#	Name	Bit Size	Description
7:5	MF	3	3-bit manufacturer ID assigned by Nokia, Bits 7:5 are 101 for Fairchild.
4:2	FW_rev	3	3-bit ascending value, indicating the firmware revision. Initial revision is 000.
1	RST_INT	1	Indicates that the device has been reset and the default values are set. 0: normal operation 1: the device has been reset and register default values are set.
0	SW_RST	1	Software reset: 0: normal operation 1: SW reset commanded

Table 4. IO Direction

- Address 03_h

Bit#	Name	Bit Size	Description
7	GPIO7	1	0: GPIO configured as input. 1: GPIO configured as output.
6	GPIO6	1	
5	GPIO5	1	
4	GPIO4	1	
3	GPIO3	1	
2	GPIO2	1	
1	GPIO1	1	
0	GPIO0	1	

Table 5. Output State

- Address 05_h
- If the pin is defined as input in register 03_h, the corresponding bit has no effect.

Bit#	Name	Bit Size	Description
7	Out 7	1	0: GPIO output = LOW. 1: GPIO output = HIGH.
6	Out 6	1	
5	Out 5	1	
4	Out 4	1	
3	Out 3	1	
2	Out 2	1	
1	Out 1	1	
0	Out 0	1	

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Table 6. Output High-Z

- Address 07_h
- If the pin is defined as input in register 03_h, the corresponding bit has no effect.

Bit#	Name	Bit Size	Description
7	Out 7	1	0: GPIO output state follows register 05_h 1: GPIO output = High-Z
6	Out 6	1	
5	Out 5	1	
4	Out 4	1	
3	Out 3	1	
2	Out 2	1	
1	Out 1	1	
0	Out 0	1	

Table 7. Input Default State

- Address 09_h
- Defines the expected state of the GPIO
- If the pin is defined as output in register 03_h, the corresponding bit has no effect.

Bit#	Name	Bit Size	Description
7	In 7	1	0: GPIO input default is set to LOW; when the GPIO goes HIGH, an interrupt is triggered. 1: GPIO input default is set to HIGH; when the GPIO goes LOW, an interrupt is triggered.
6	In 6	1	
5	In 5	1	
4	In 4	1	
3	In 3	1	
2	In 2	1	
1	In 1	1	
0	In 0	1	

Table 8. Pull Enable

- Address $0B_h$
- Pull enable for input pin
- If the pin is defined as output in register 03_h, the corresponding bit has no effect.

Bit#	Name	Bit Size	Description
7	In 7	1	0: GPIO input pull-up/pull-down is not enabled. 1: GPIO input Pull-up/Pull-down is enabled.
6	In 6	1	
5	In 5	1	
4	In 4	1	
3	In 3	1	
2	In 2	1	
1	In 1	1	
0	In 0	1	

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Table 9. Pull-Down / Pull-Up

- Address $0D_h$
- If the pin is defined as output in register 03_h, the corresponding bit has no effect.
- If the corresponding bit in register $0B_h$=0, this register setting has no effect.

Bit#	Name	Bit Size	Description
7	In 7	1	0: GPIO input pull-down is enabled. 1: GPIO input pull-up is enabled.
6	In 6	1	
5	In 5	1	
4	In 4	1	
3	In 3	1	
2	In 2	1	
1	In 1	1	
0	In 0	1	

Table 10. Input Status

- Address $0F_h$
- If the pin is defined as output in register 03_h, the corresponding bit has no effect.
- This bit shows the real-time input pin status.

Bit#	Name	Bit Size	Description
7	In 7	1	0: GPIO input is LOW. 1: GPIO input is HIGH.
6	In 6	1	
5	In 5	1	
4	In 4	1	
3	In 3	1	
2	In 2	1	
1	In 1	1	
0	In 0	1	

Table 11. Interrupt Mask

- Address 11_h
- If the pin is defined as output in register 03_h, the corresponding bit has no effect.
- This bit enables the interrupt generation from input pin state change to INT.

Bit#	Name	Bit Size	Description
7	In 7	1	0: GPIO input interrupt is generated. 1: GPIO input interrupt is masked.
6	In 6	1	
5	In 5	1	
4	In 4	1	
3	In 3	1	
2	In 2	1	
1	In 1	1	
0	In 0	1	

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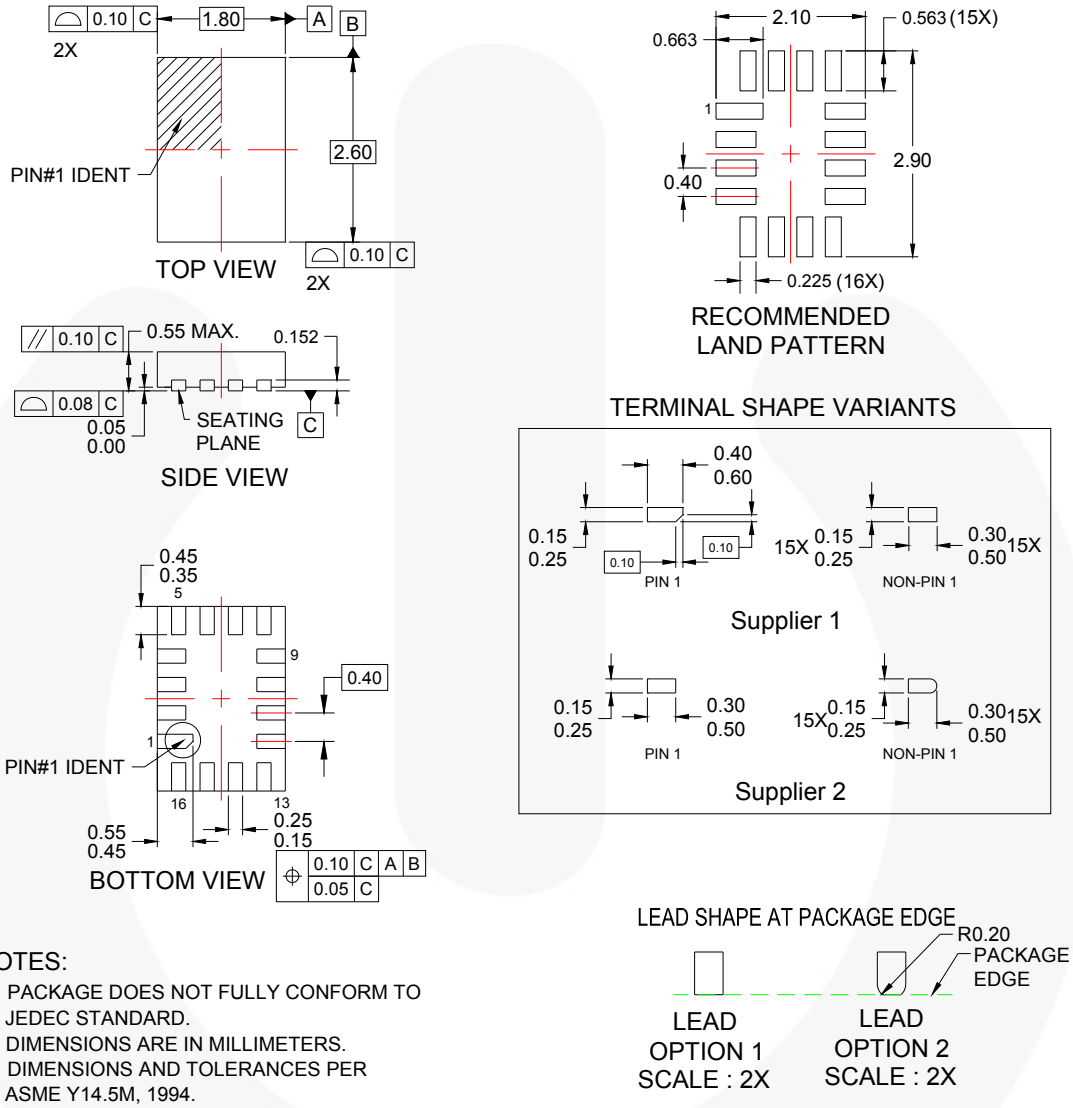
Table 12. Interrupt Status

- Address 13_h
- This bit is HIGH if input GPIO ≠ default state (register 09h).
- The flag is cleared after being read by the master (bit returns to 0).
- The input must go back to default state and change again before this flag is raised again.

Bit#	Name	Bit Size	Description
7	In 7	1	0: GPIO input is in default state or the flag has been cleared. 1: GPIO input has changed state from default.
6	In 6	1	
5	In 5	1	
4	In 4	1	
3	In 3	1	
2	In 2	1	
1	In 1	1	
0	In 0	1	

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Physical Dimensions



NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC STANDARD.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
D. LAND PATTERN RECOMMENDATION IS BASED ON FSC DESIGN ONLY.
E. DRAWING FILENAME: MKT-UMLP16Arev4.
F. TERMINAL SHAPE MAY VARY ACCORDING TO PACKAGE SUPPLIER, SEE TERMINAL SHAPE VARIANTS.

Figure 10. 16-lead, UMLP, QUAD, Ultra-Thin MLP, 1.8 x 2.6 mm

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