

# SBC-A62-J Reference Schematics

## DISCLAIMER

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## Reference Table

Capacitors CC (Ceramic), CE (Electrolytic):  
After the value, it is shown the Minimum Rated Voltage (MRV).  
If this it is not shown, then it is implicit that MRV is 6.3V.  
Components with /X indications are foreseen in the PCB but must not be mounted  
Components with CFG indications are factory alternatives for the mounting

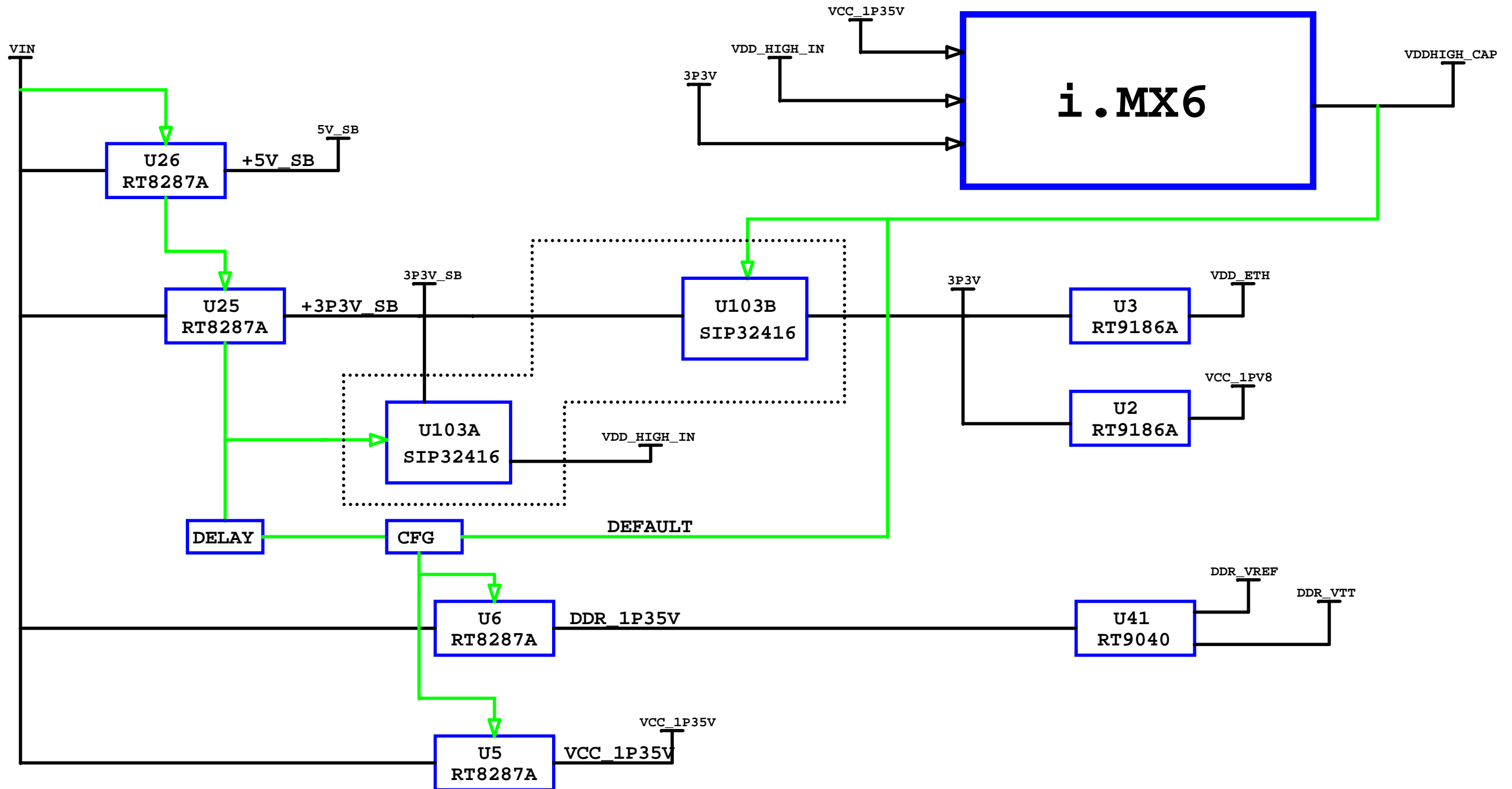
## RECOMMENDED OPERATING CONDITIONS

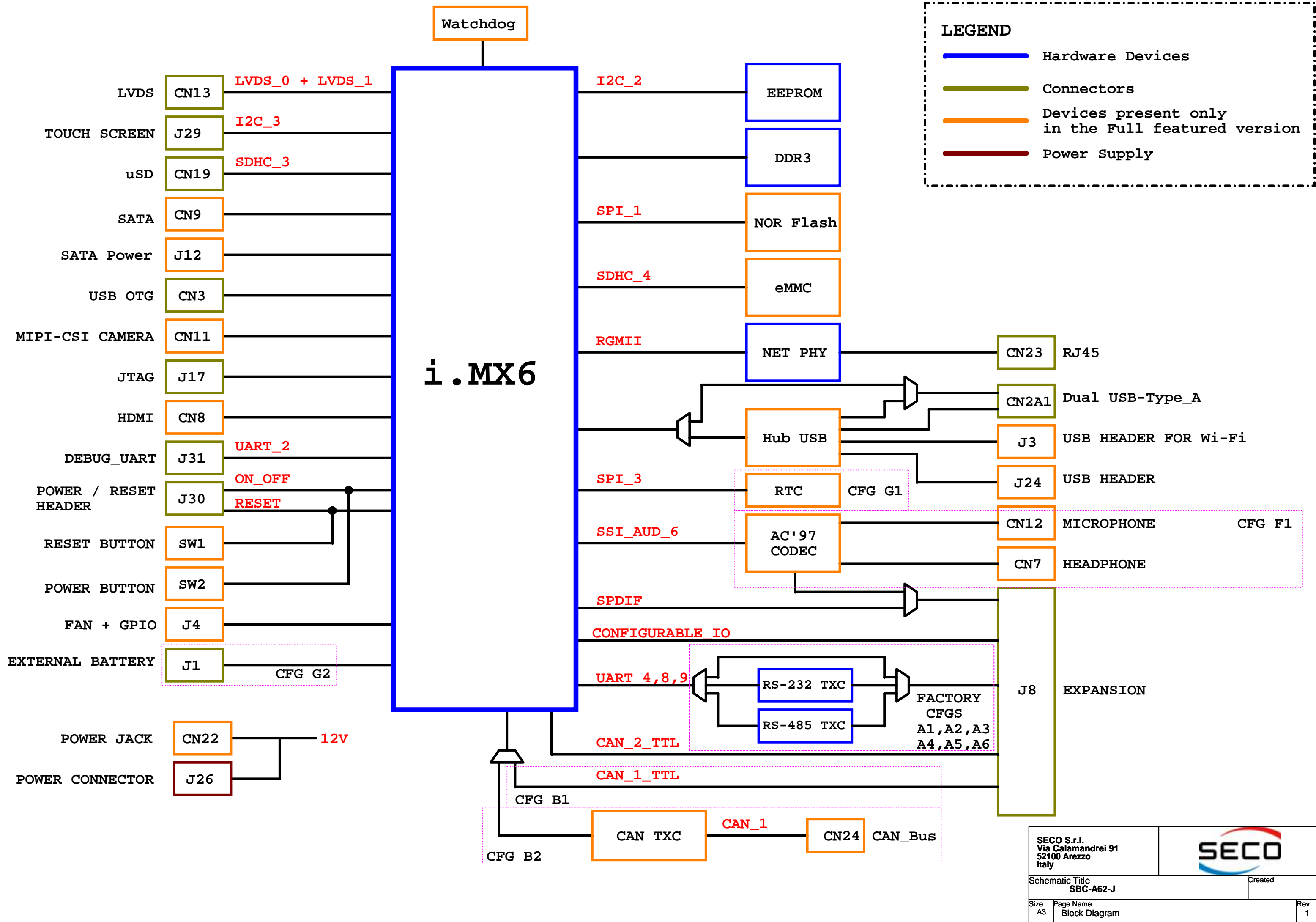
Supply voltage.....12V ± 10%

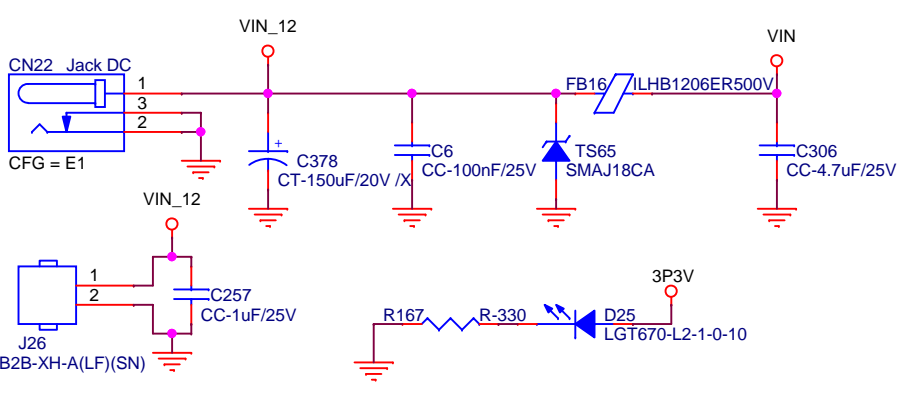
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Green-highlighted signals are regulators' enabling signals.

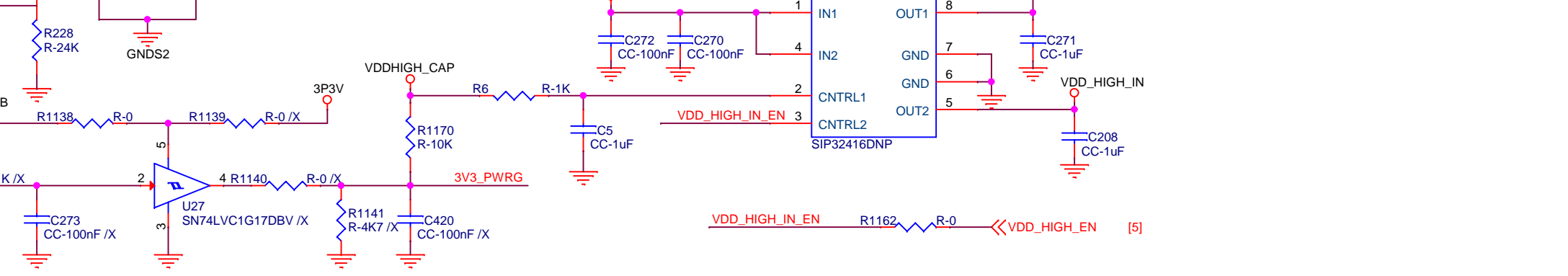
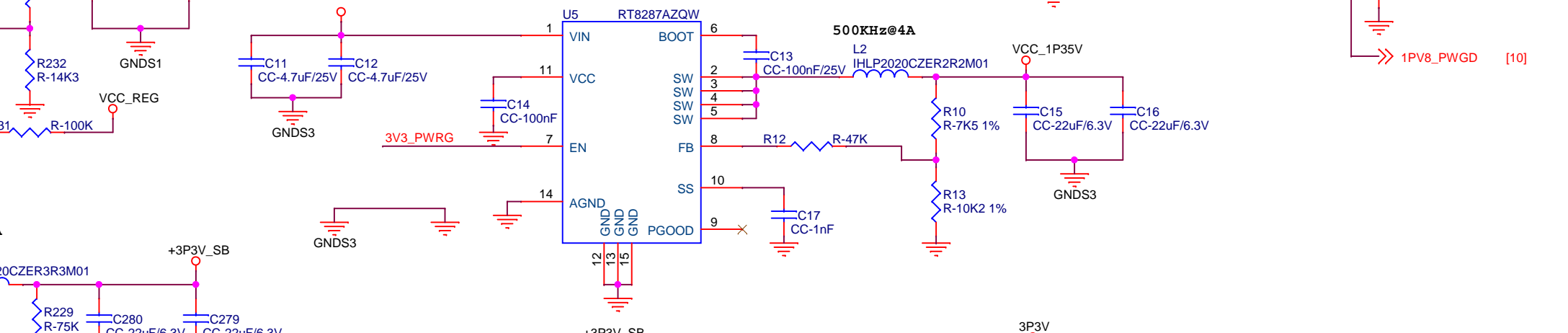
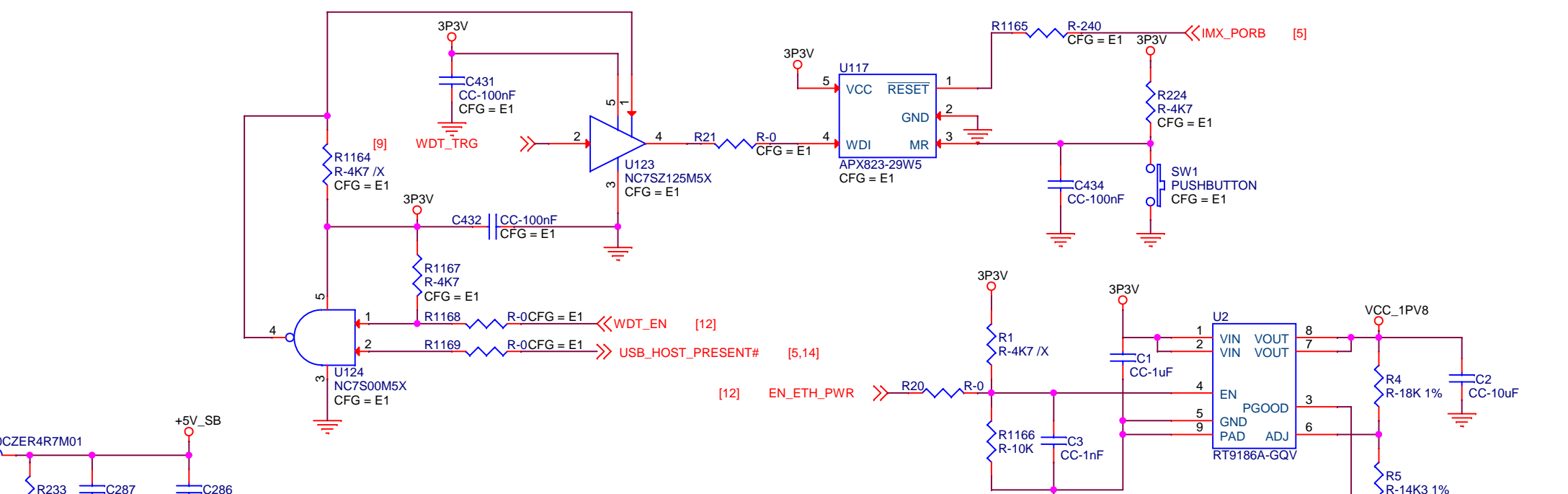
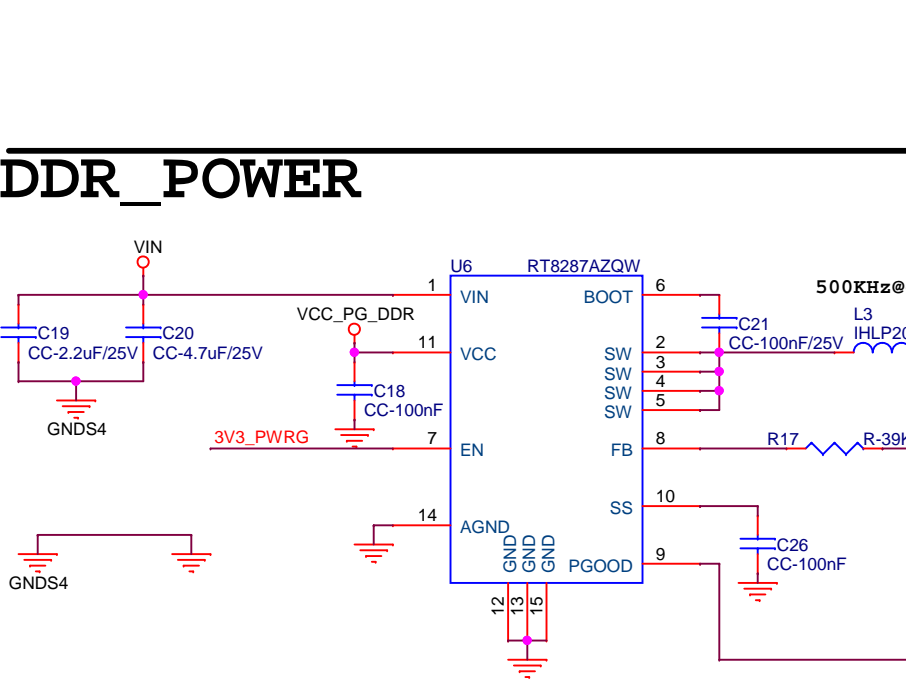
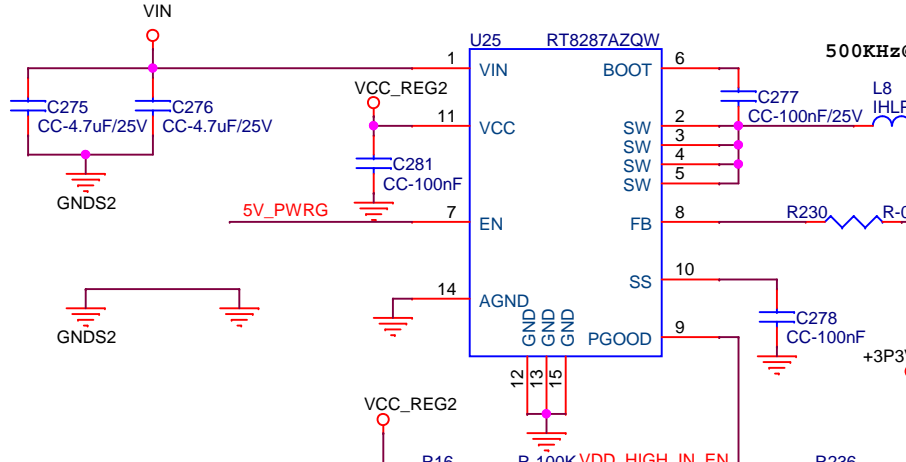
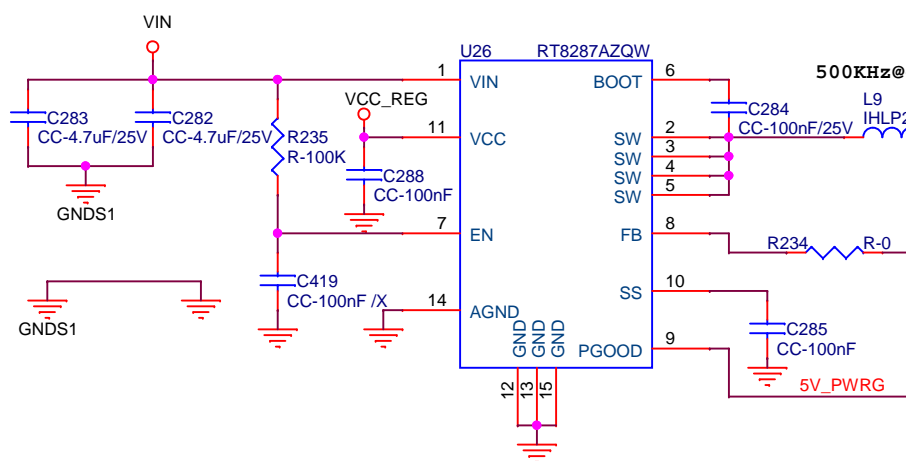
In the diagram below, the horizontal position of each regulator is indicative of the instant when the regulator is enabled with respect to the moment when the board is powered on.



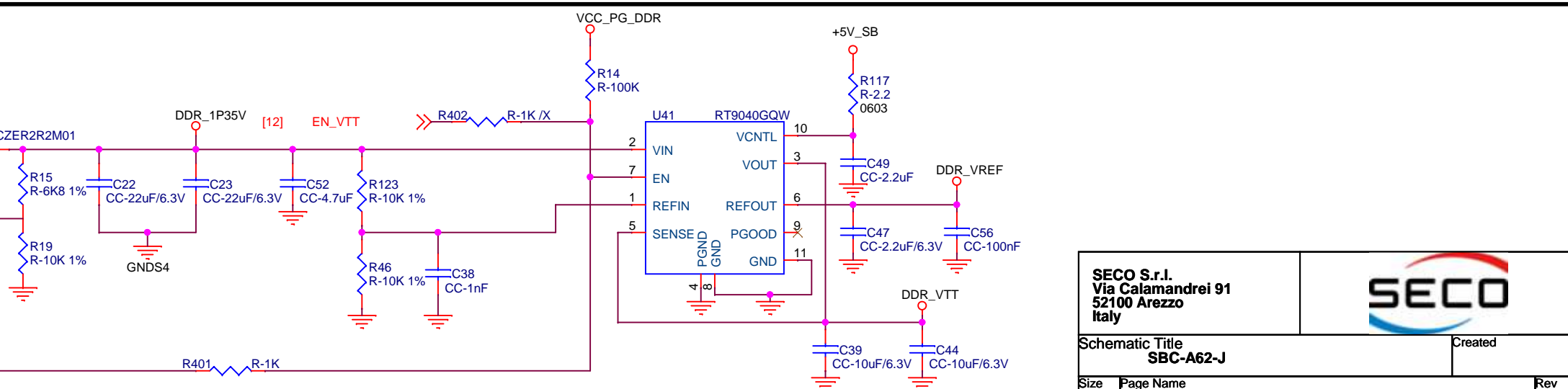
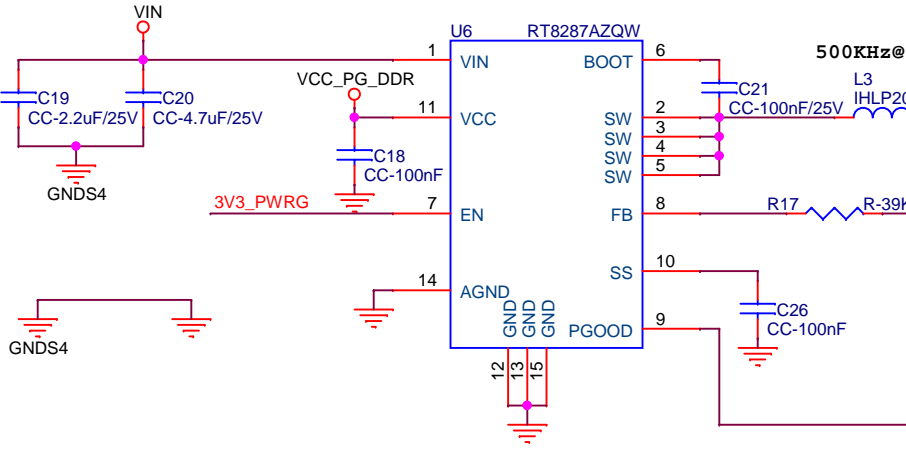


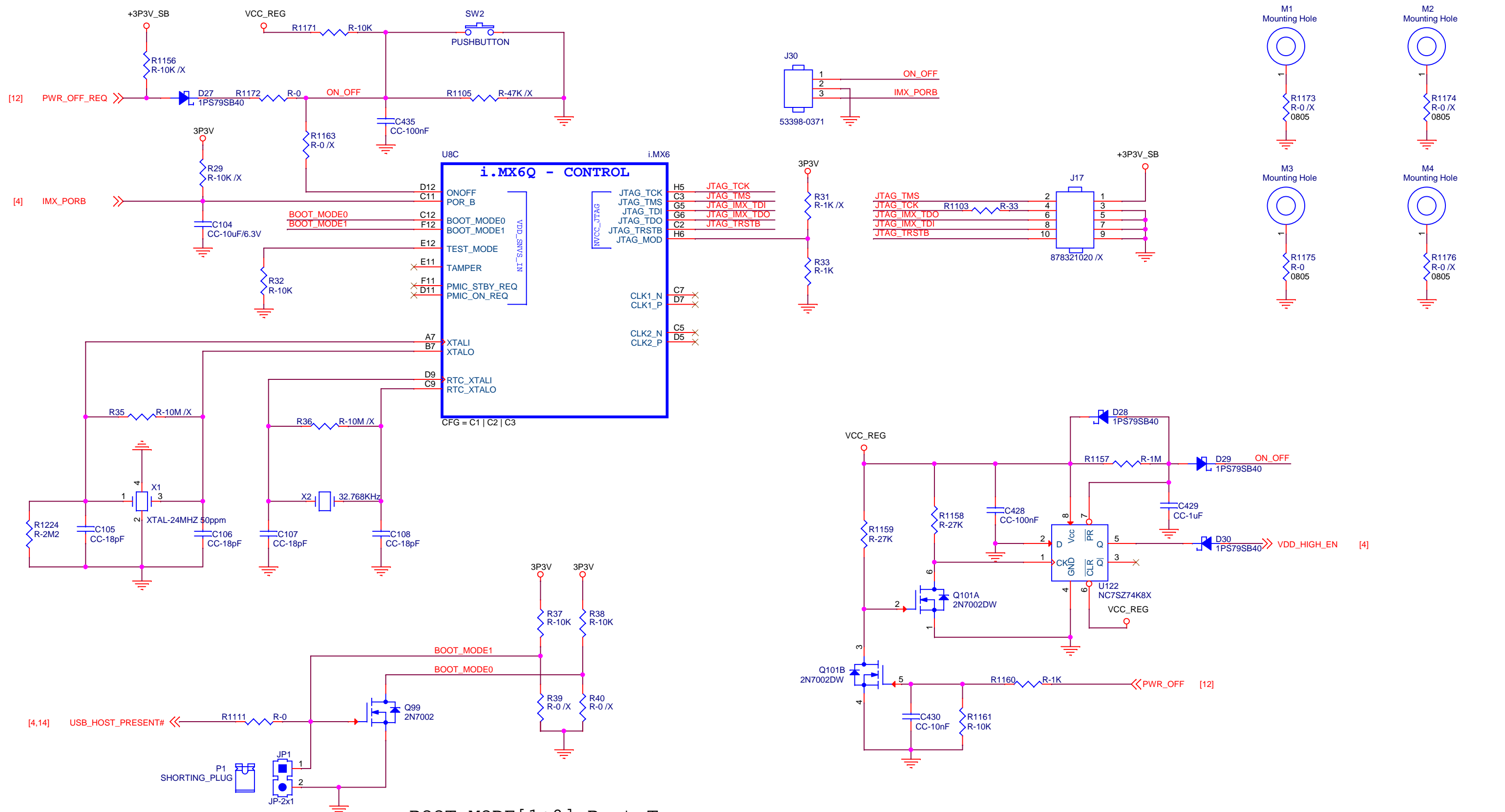


**12 VDC POWER SUPPLY**



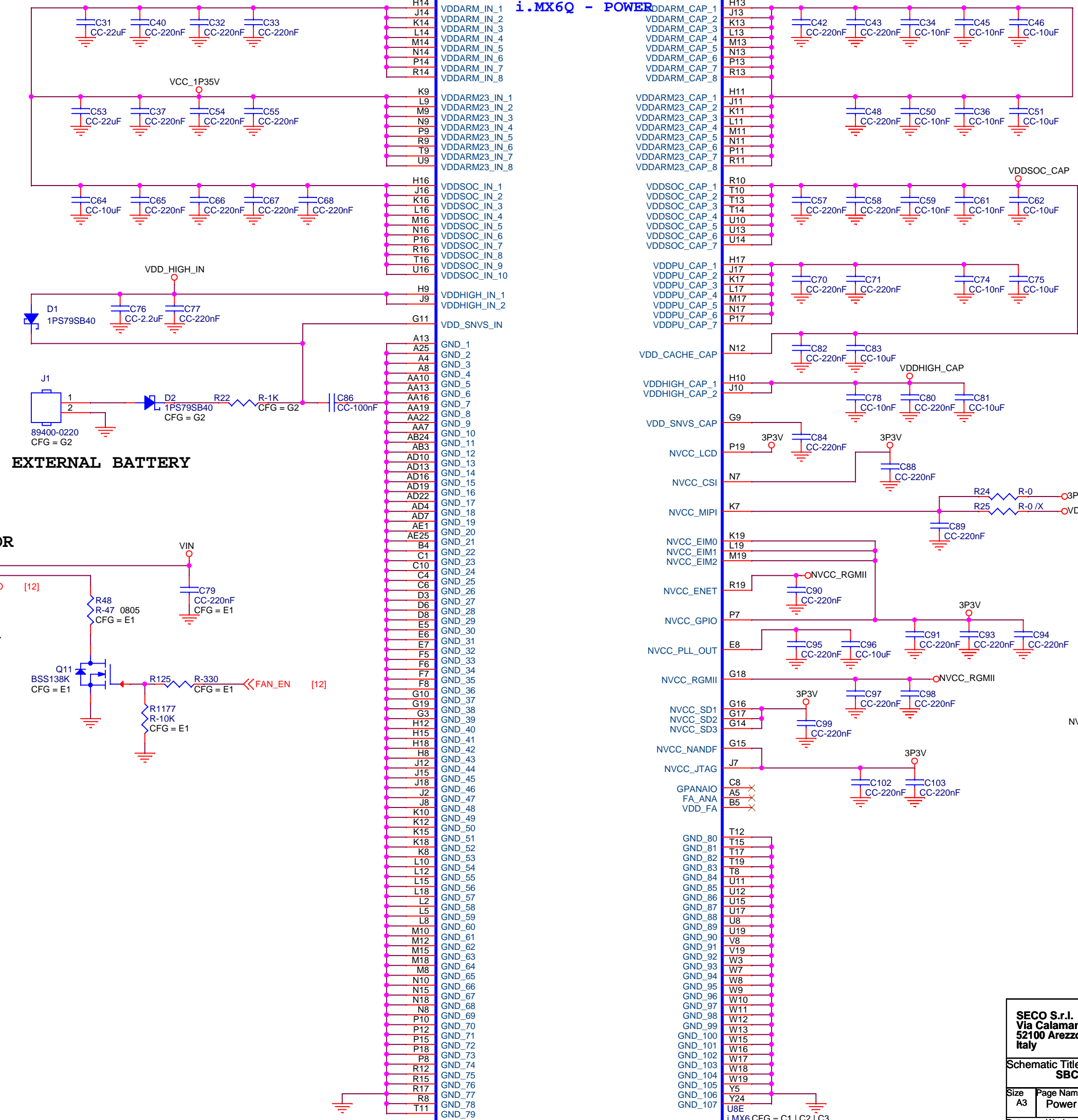
**DDR\_POWER**



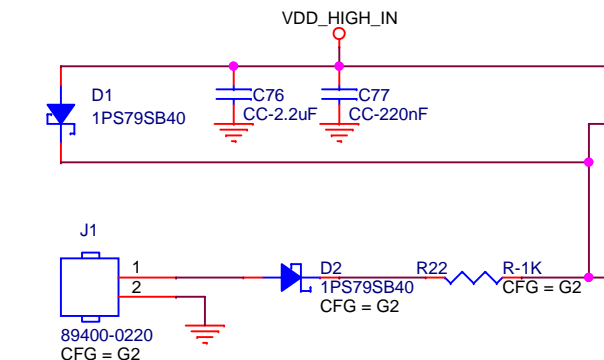


BOOT\_MODE[1:0] Boot Type  
 01 Serial Downloader  
 10 Internal Boot

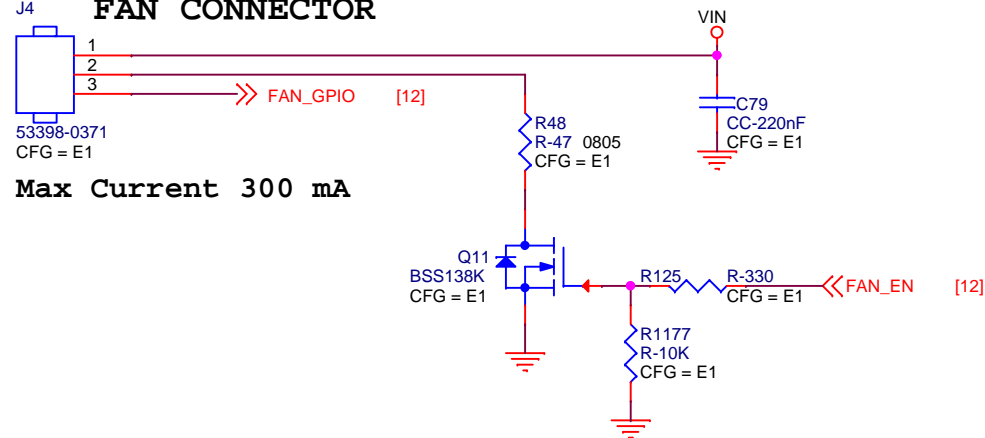
# i.MX6Q - POWER



## EXTERNAL BATTERY



## FAN CONNECTOR



- H14 VDDARM\_IN\_1
- J14 VDDARM\_IN\_2
- K14 VDDARM\_IN\_3
- L14 VDDARM\_IN\_4
- M14 VDDARM\_IN\_5
- N14 VDDARM\_IN\_6
- P14 VDDARM\_IN\_7
- R14 VDDARM\_IN\_8
- K9 VDDARM23\_IN\_1
- L9 VDDARM23\_IN\_2
- M9 VDDARM23\_IN\_3
- N9 VDDARM23\_IN\_4
- P9 VDDARM23\_IN\_5
- R9 VDDARM23\_IN\_6
- T9 VDDARM23\_IN\_7
- U9 VDDARM23\_IN\_8
- H16 VDDSOC\_IN\_1
- J16 VDDSOC\_IN\_2
- K16 VDDSOC\_IN\_3
- L16 VDDSOC\_IN\_4
- M16 VDDSOC\_IN\_5
- N16 VDDSOC\_IN\_6
- P16 VDDSOC\_IN\_7
- R16 VDDSOC\_IN\_8
- T16 VDDSOC\_IN\_9
- U16 VDDSOC\_IN\_10
- H9 VDDHIGH\_IN\_1
- J9 VDDHIGH\_IN\_2
- G11 VDD\_SNVS\_IN
- A13 GND\_1
- A25 GND\_2
- A4 GND\_3
- A8 GND\_4
- AA10 GND\_5
- AA13 GND\_6
- AA16 GND\_7
- AA19 GND\_8
- AA22 GND\_9
- AA7 GND\_10
- AB24 GND\_11
- AB3 GND\_12
- AD10 GND\_13
- AD13 GND\_14
- AD16 GND\_15
- AD19 GND\_16
- AD22 GND\_17
- AD4 GND\_18
- AD7 GND\_19
- AE1 GND\_20
- AE25 GND\_21
- B4 GND\_22
- C1 GND\_23
- C10 GND\_24
- C4 GND\_25
- C6 GND\_26
- D3 GND\_27
- D6 GND\_28
- D8 GND\_29
- E5 GND\_30
- E6 GND\_31
- E7 GND\_32
- F5 GND\_33
- F6 GND\_34
- F7 GND\_35
- F8 GND\_36
- G10 GND\_37
- G19 GND\_38
- G3 GND\_39
- H12 GND\_40
- H15 GND\_41
- H18 GND\_42
- H8 GND\_43
- J12 GND\_44
- J15 GND\_45
- J18 GND\_46
- J2 GND\_47
- J8 GND\_48
- K10 GND\_49
- K12 GND\_50
- K15 GND\_51
- K18 GND\_52
- K8 GND\_53
- L10 GND\_54
- L12 GND\_55
- L15 GND\_56
- L18 GND\_57
- L2 GND\_58
- L5 GND\_59
- L8 GND\_60
- M10 GND\_61
- M12 GND\_62
- M15 GND\_63
- M18 GND\_64
- M8 GND\_65
- N10 GND\_66
- N15 GND\_67
- N18 GND\_68
- N8 GND\_69
- P10 GND\_70
- P12 GND\_71
- P15 GND\_72
- P18 GND\_73
- P8 GND\_74
- R12 GND\_75
- R15 GND\_76
- R17 GND\_77
- R8 GND\_78
- T11 GND\_79

- H13 VDDARM\_CAP\_1
- J13 VDDARM\_CAP\_2
- K13 VDDARM\_CAP\_3
- L13 VDDARM\_CAP\_4
- M13 VDDARM\_CAP\_5
- N13 VDDARM\_CAP\_6
- P13 VDDARM\_CAP\_7
- R13 VDDARM\_CAP\_8
- H11 VDDARM23\_CAP\_1
- J11 VDDARM23\_CAP\_2
- K11 VDDARM23\_CAP\_3
- L11 VDDARM23\_CAP\_4
- M11 VDDARM23\_CAP\_5
- N11 VDDARM23\_CAP\_6
- P11 VDDARM23\_CAP\_7
- R11 VDDARM23\_CAP\_8
- R10 VDDSOC\_CAP\_1
- T10 VDDSOC\_CAP\_2
- T13 VDDSOC\_CAP\_3
- T14 VDDSOC\_CAP\_4
- U10 VDDSOC\_CAP\_5
- U13 VDDSOC\_CAP\_6
- U14 VDDSOC\_CAP\_7
- H17 VDDPU\_CAP\_1
- J17 VDDPU\_CAP\_2
- K17 VDDPU\_CAP\_3
- L17 VDDPU\_CAP\_4
- M17 VDDPU\_CAP\_5
- N17 VDDPU\_CAP\_6
- P17 VDDPU\_CAP\_7
- N12 VDDCACHE\_CAP\_1
- H10 VDDHIGH\_CAP\_1
- J10 VDDHIGH\_CAP\_2
- G9 VDDSNV\_CAP\_1
- P19 NVCC\_LCD
- N7 NVCC\_CSI
- K7 NVCC\_MIPI
- K19 NVCC\_EIM0
- L19 NVCC\_EIM1
- M19 NVCC\_EIM2
- R19 NVCC\_ENET
- P7 NVCC\_GPIO
- E8 NVCC\_PLL\_OUT
- G18 NVCC\_RGMII
- G16 NVCC\_SD1
- G17 NVCC\_SD2
- G14 NVCC\_SD3
- G15 NVCC\_NANDF
- J7 NVCC\_JTAG
- C8 GPANAIO
- A5 FA\_ANA
- B5 VDD\_FA
- T12 GND\_80
- T15 GND\_81
- T17 GND\_82
- T19 GND\_83
- T8 GND\_84
- U11 GND\_85
- U12 GND\_86
- U15 GND\_87
- U17 GND\_88
- U8 GND\_89
- U19 GND\_90
- V8 GND\_91
- V19 GND\_92
- W3 GND\_93
- W7 GND\_94
- W8 GND\_95
- W9 GND\_96
- W10 GND\_97
- W11 GND\_98
- W12 GND\_99
- W13 GND\_100
- W15 GND\_101
- W16 GND\_102
- W17 GND\_103
- W18 GND\_104
- W19 GND\_105
- Y5 GND\_106
- Y24 GND\_107
- U8E GND\_108

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i.MX6 CFG = C1 | C2 | C3

i.MX6Q - DDR

DRAM_D0	AD2
DRAM_D1	AE2
DRAM_D2	AC4
DRAM_D3	AA5
DRAM_D4	AC1
DRAM_D5	AD1
DRAM_D6	AB4
DRAM_D7	AE4
DRAM_SDQS0	AE3
DRAM_SDQS0_B	AD3
DRAM_DQM0	AC3

DRAM_D8	AD5
DRAM_D9	AE5
DRAM_D10	AA6
DRAM_D11	AE7
DRAM_D12	AB5
DRAM_D13	AC5
DRAM_D14	AB6
DRAM_D15	AC7
DRAM_SDQS1	AD6
DRAM_SDQS1_B	AE6
DRAM_DQM1	AC6

DRAM_D16	AB7
DRAM_D17	AA8
DRAM_D18	AB9
DRAM_D19	Y9
DRAM_D20	Y7
DRAM_D21	Y8
DRAM_D22	AC8
DRAM_D23	AA9
DRAM_SDQS2	AD8
DRAM_SDQS2_B	AE8
DRAM_DQM2	AB8

DRAM_D24	AE9
DRAM_D25	Y10
DRAM_D26	AE11
DRAM_D27	AB11
DRAM_D28	AC9
DRAM_D29	AD9
DRAM_D30	AD11
DRAM_D31	AC11
DRAM_SDQS3	AC10
DRAM_SDQS3_B	AB10
DRAM_DQM3	AE10

DRAM_D32	AA17
DRAM_D33	AA18
DRAM_D34	AC18
DRAM_D35	AE19
DRAM_D36	Y17
DRAM_D37	Y18
DRAM_D38	AB19
DRAM_D39	AC19
DRAM_SDQS4	AD18
DRAM_SDQS4_B	AE18
DRAM_DQM4	AB18

DRAM_D40	Y19
DRAM_D41	AB20
DRAM_D42	AB21
DRAM_D43	AD21
DRAM_D44	Y20
DRAM_D45	AA20
DRAM_D46	AE21
DRAM_D47	AC21
DRAM_SDQS5	AD20
DRAM_SDQS5_B	AE20
DRAM_DQM5	AC20

DRAM_D48	AC22
DRAM_D49	AE22
DRAM_D50	AE24
DRAM_D51	AC24
DRAM_D52	AB22
DRAM_D53	AC23
DRAM_D54	AD25
DRAM_D55	AC25
DRAM_SDQS6	AD23
DRAM_SDQS6_B	AE23
DRAM_DQM6	AD24

DRAM_D56	AB25
DRAM_D57	AA21
DRAM_D58	Y25
DRAM_D59	Y22
DRAM_D60	AB23
DRAM_D61	AA23
DRAM_D62	Y23
DRAM_D63	W25
DRAM_SDQS7	AA25
DRAM_SDQS7_B	AA24
DRAM_DQM7	Y21

U8J i.MX6

CFG = C1 | C2 | C3

DRAM_A0	AC14
DRAM_A1	AB14
DRAM_A2	AA14
DRAM_A3	Y14
DRAM_A4	W14
DRAM_A5	AE13
DRAM_A6	AC13
DRAM_A7	Y13
DRAM_A8	AB13
DRAM_A9	AE12
DRAM_A10	AA15
DRAM_A11	AC12
DRAM_A12	AD12
DRAM_A13	AC17
DRAM_A14	AA12
DRAM_A15	Y12

DRAM_SDBA0	AC15
DRAM_SDBA1	Y15
DRAM_SDBA2	AB12

DRAM_CS0	Y16
DRAM_CS1	AD17

DRAM_RAS	AB15
DRAM_CAS	AE16
DRAM_SDWE	AB16

DRAM_SDCKE0	Y11
DRAM_SDCKE1	AA11

DRAM_SDODT0	AC16
DRAM_SDODT1	AB17

DRAM_RESET	Y6
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DRAM_SDCLK_0	AD15
DRAM_SDCLK_0_B	AE15

DRAM_SDCLK_1	AD14
DRAM_SDCLK_1_B	AE14

DRAM_VREF	AC2
-----------	-----

ZQPAD	AE17
-------	------

NVCC_DRAM_1	R18
NVCC_DRAM_2	T18
NVCC_DRAM_3	U18
NVCC_DRAM_4	V10
NVCC_DRAM_5	V11
NVCC_DRAM_6	V12
NVCC_DRAM_7	V13
NVCC_DRAM_8	V14
NVCC_DRAM_9	V15
NVCC_DRAM_10	V16
NVCC_DRAM_11	V17
NVCC_DRAM_12	V18
NVCC_DRAM_13	V9

DRAM_A0	[8]
DRAM_A1	[8]
DRAM_A2	[8]
DRAM_A3	[8]
DRAM_A4	[8]
DRAM_A5	[8]
DRAM_A6	[8]
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DRAM_CS0_B	[8]
DRAM_RAS_B	[8]
DRAM_CAS_B	[8]
DRAM_WE_B	[8]

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DRAM_SDODT1	[8]

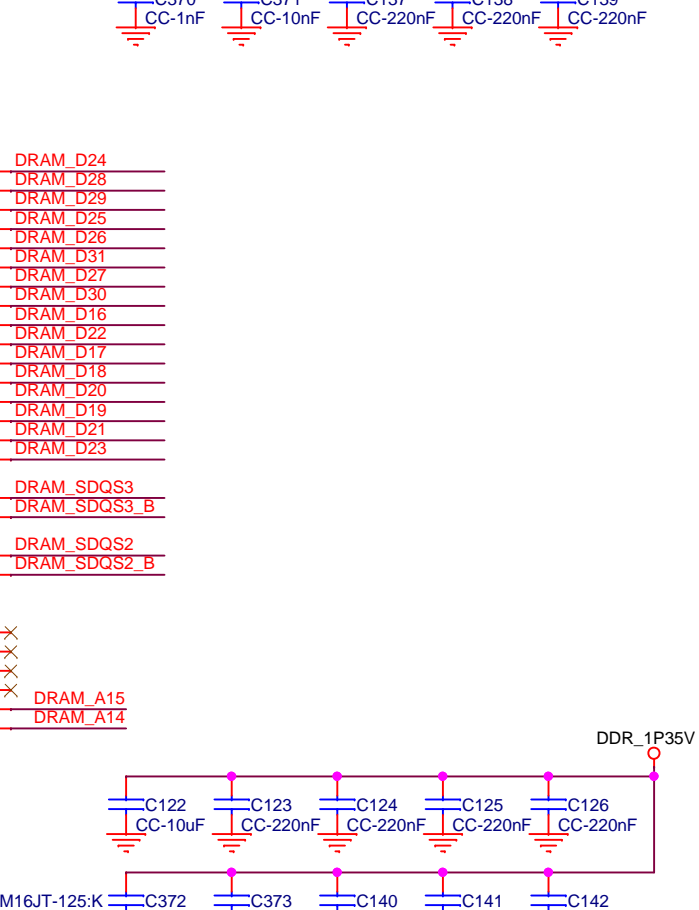
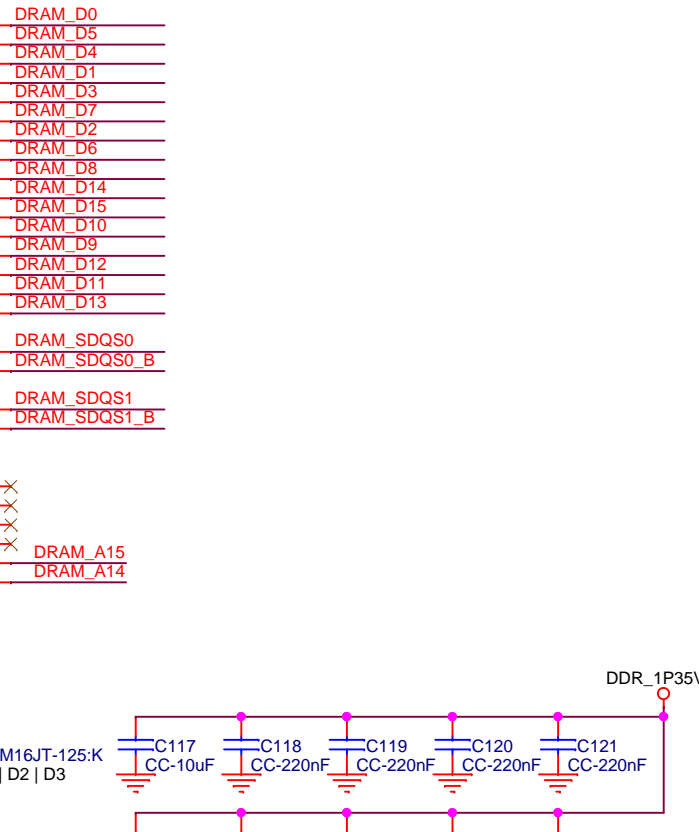
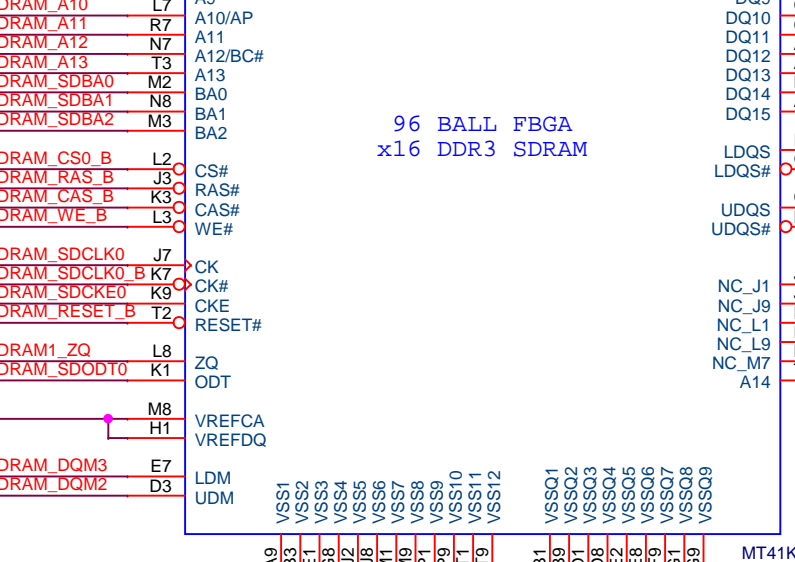
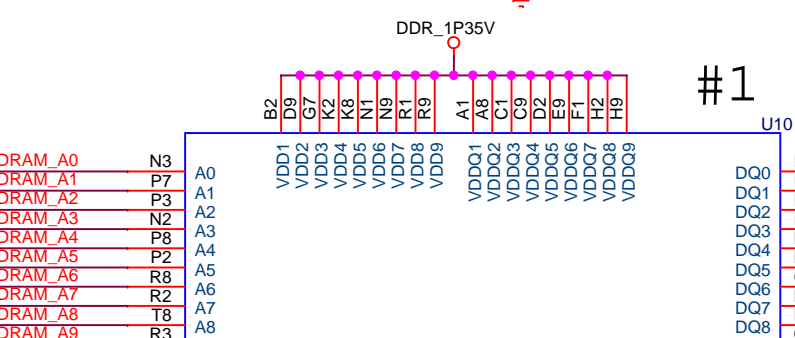
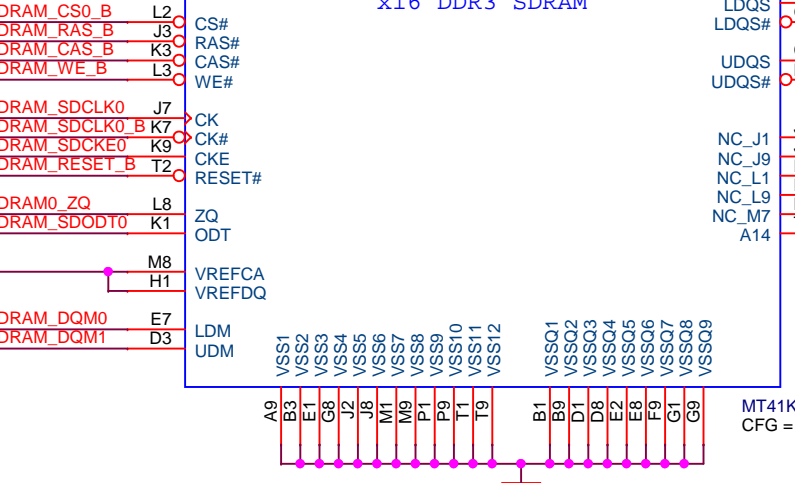
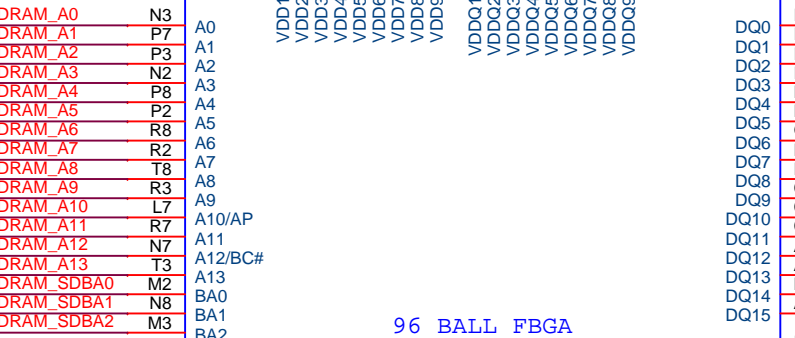
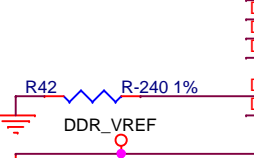
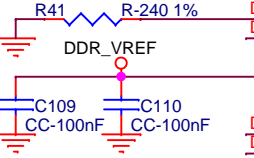
DRAM_RESET_B	[8]
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DRAM_SDCLK0	[8]
DRAM_SDCLK0_B	[8]

DRAM_VREF	[8]
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ZQPAD	[8]
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NVCC_DRAM_1	[8]
NVCC_DRAM_2	[8]
NVCC_DRAM_3	[8]
NVCC_DRAM_4	[8]
NVCC_DRAM_5	[8]
NVCC_DRAM_6	[8]
NVCC_DRAM_7	[8]
NVCC_DRAM_8	[8]
NVCC_DRAM_9	[8]
NVCC_DRAM_10	[8]
NVCC_DRAM_11	[8]
NVCC_DRAM_12	[8]
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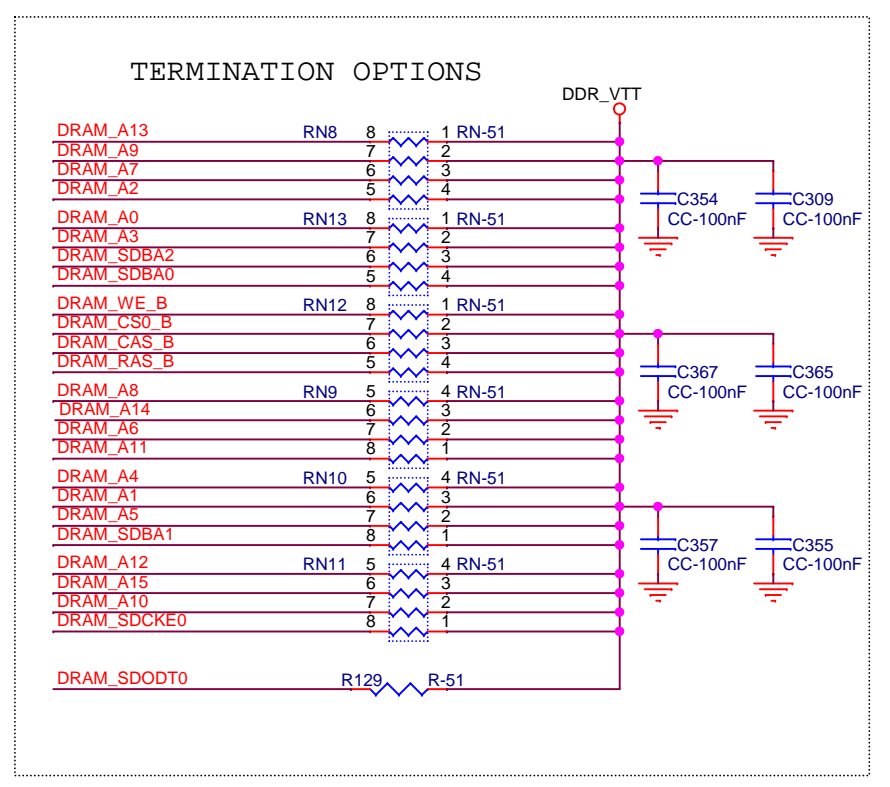
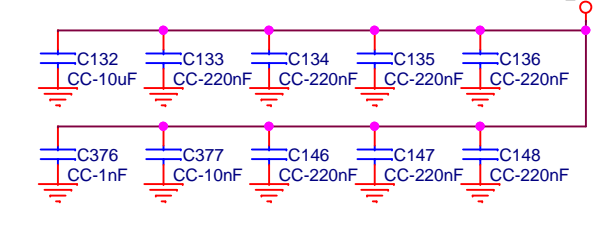
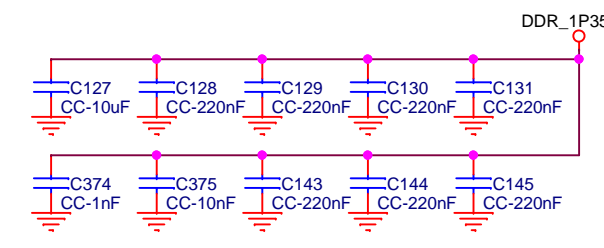
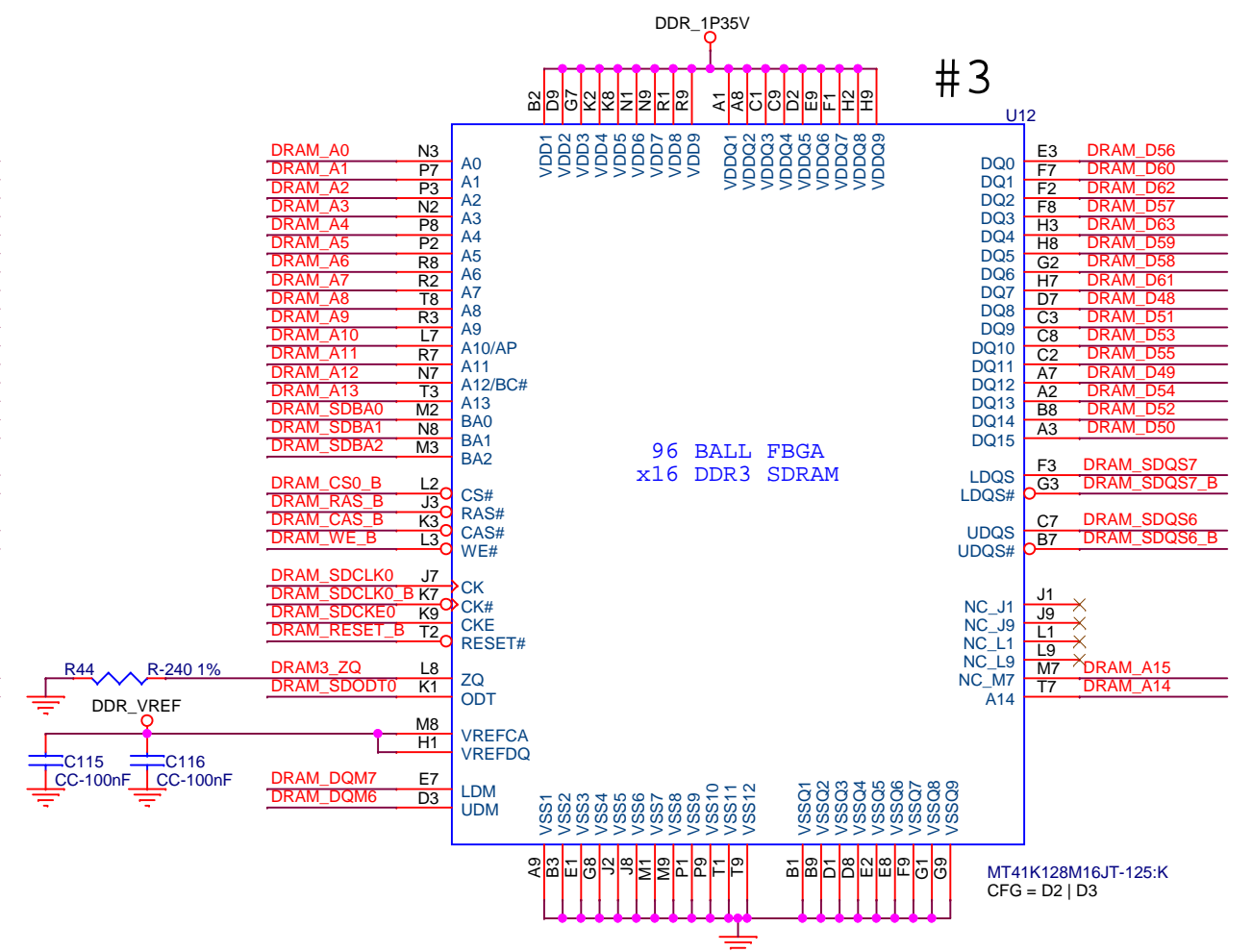
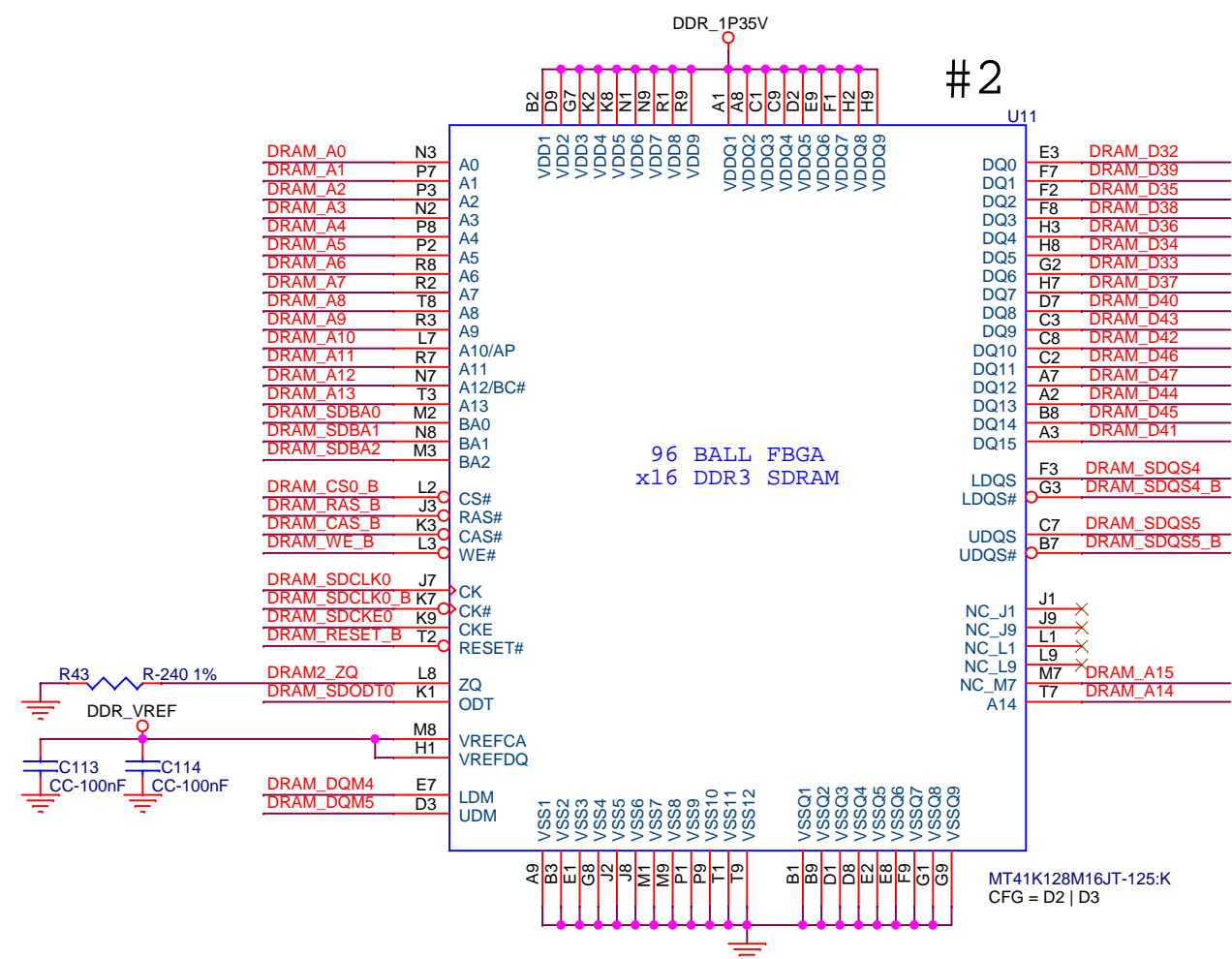
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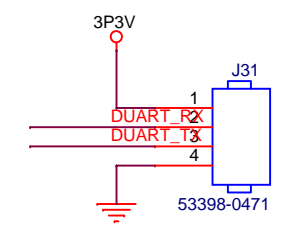
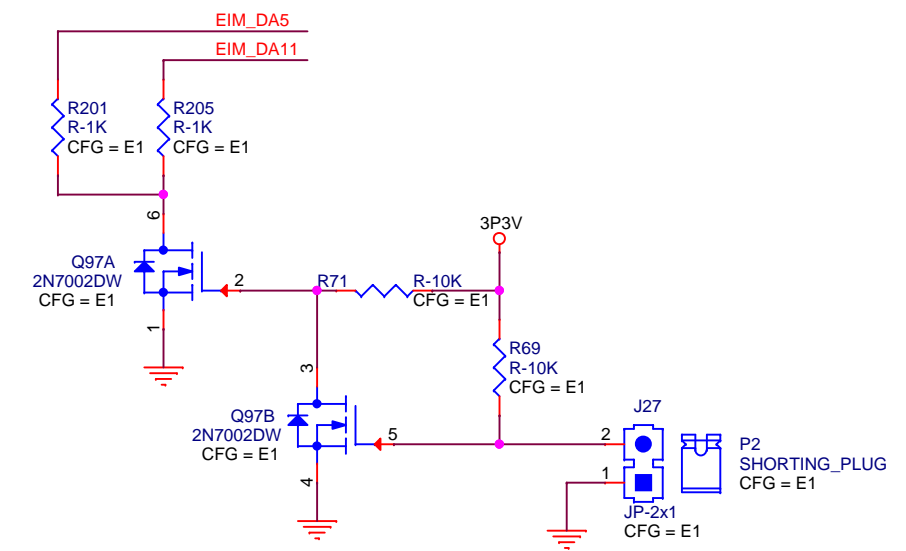
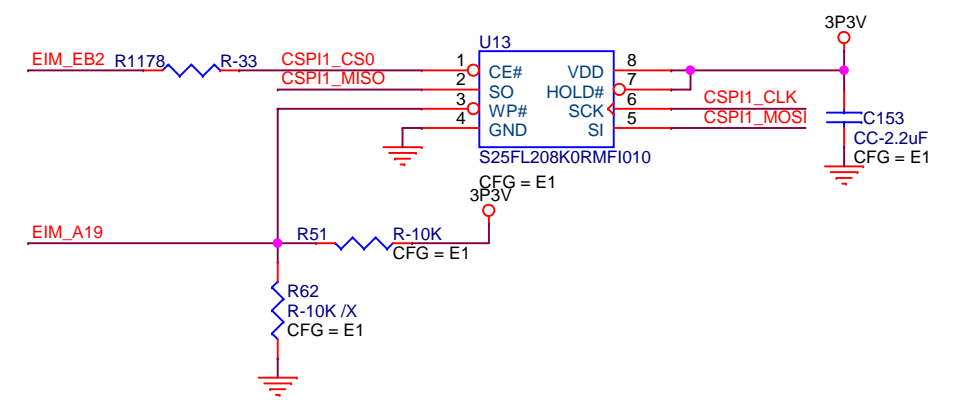
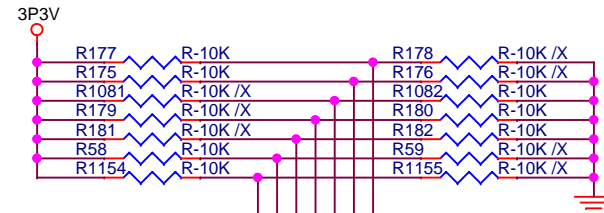
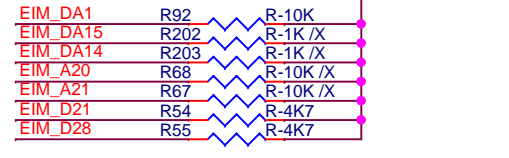
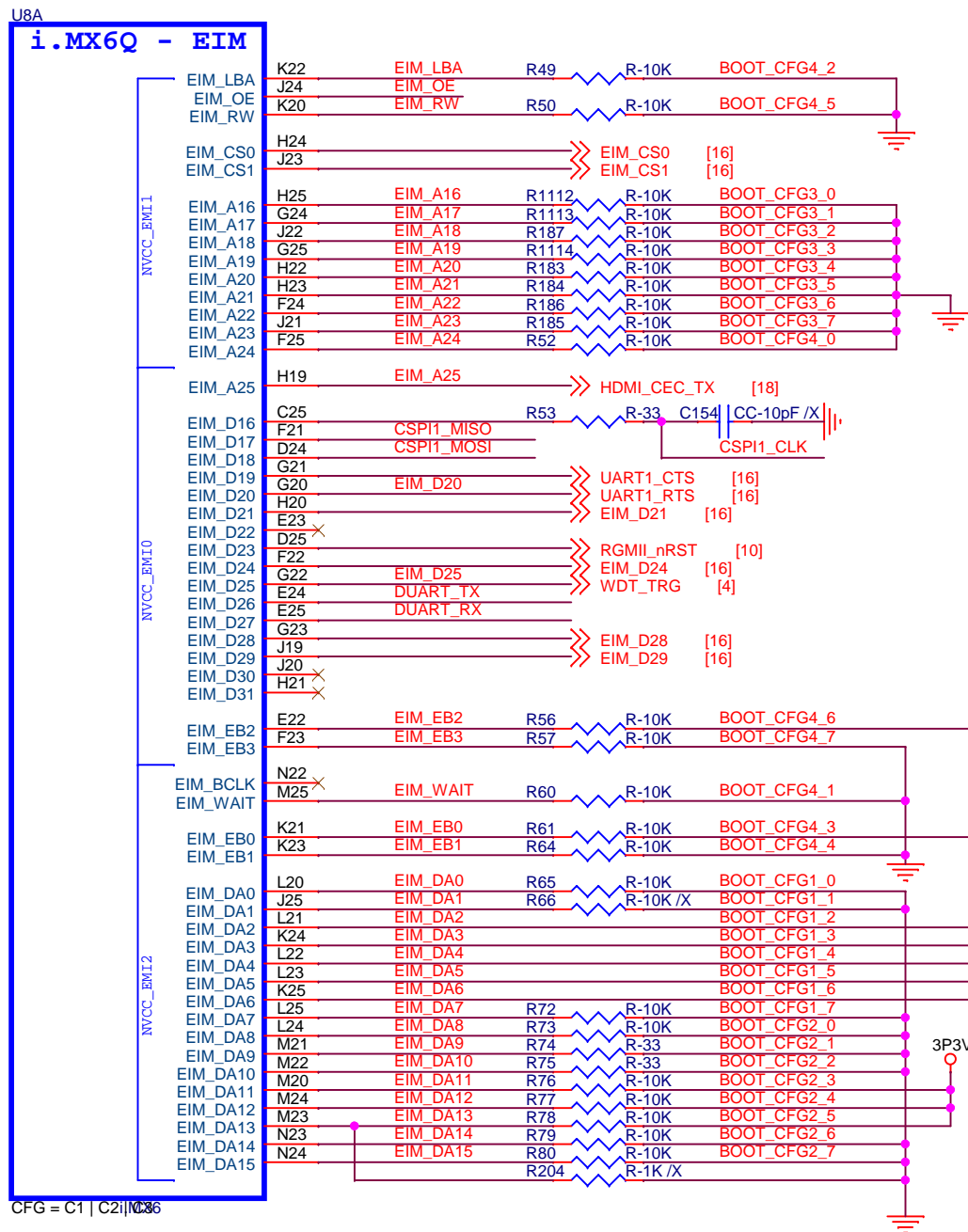
Size: A3 Page Name: DDR3- Lower 32 bit Rev: 1

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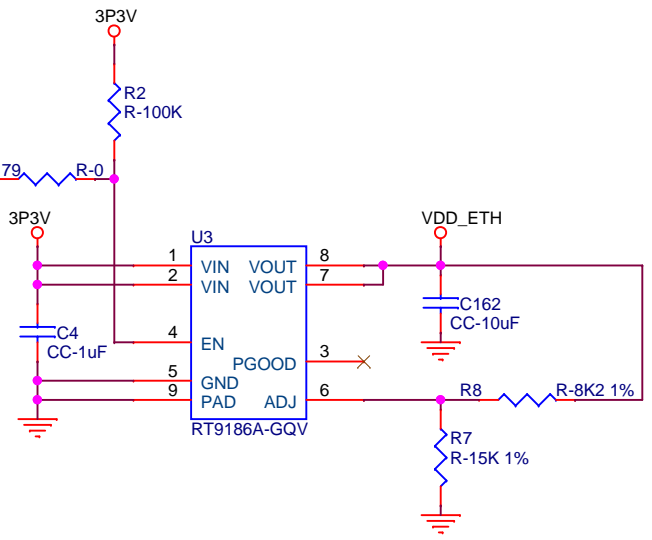
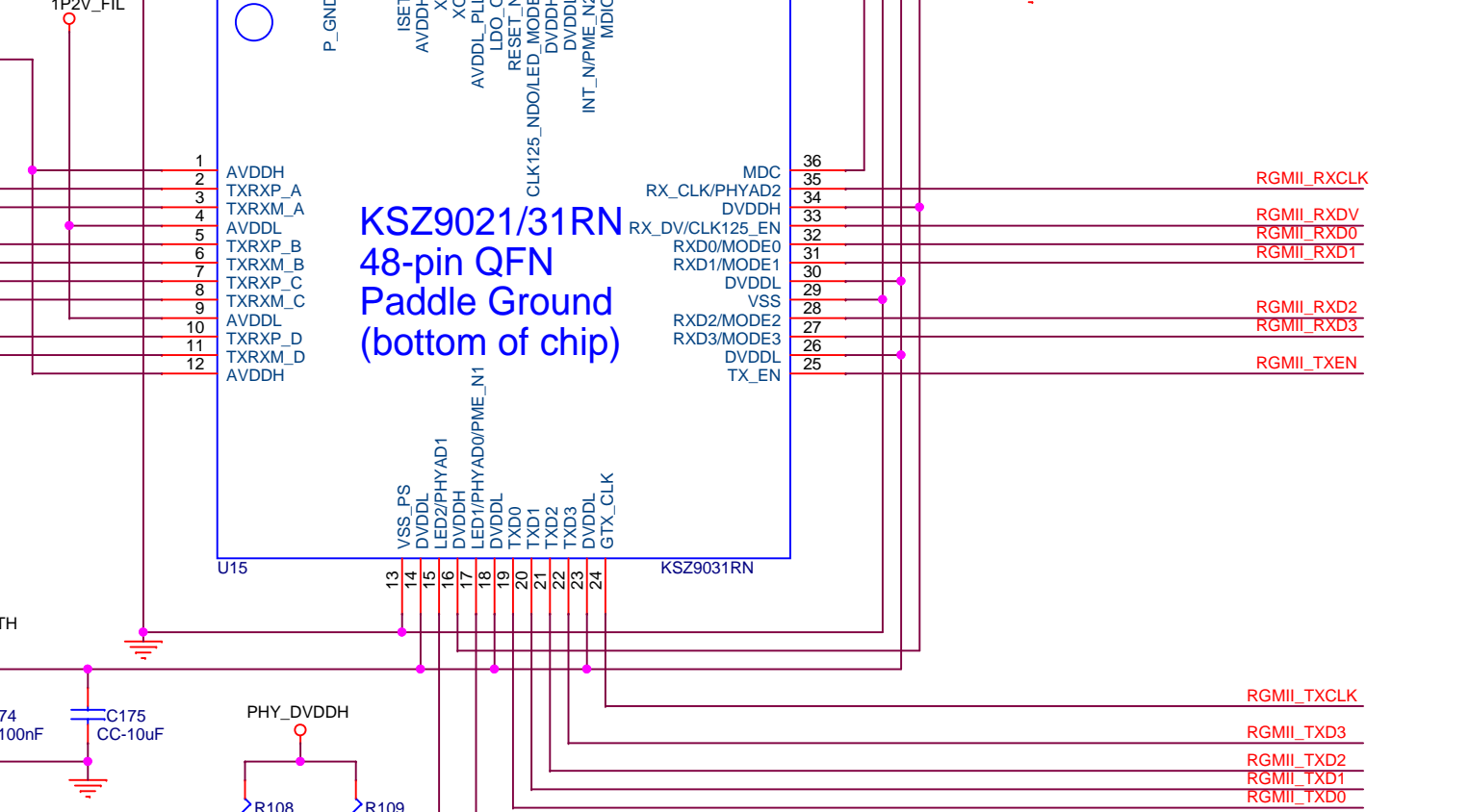
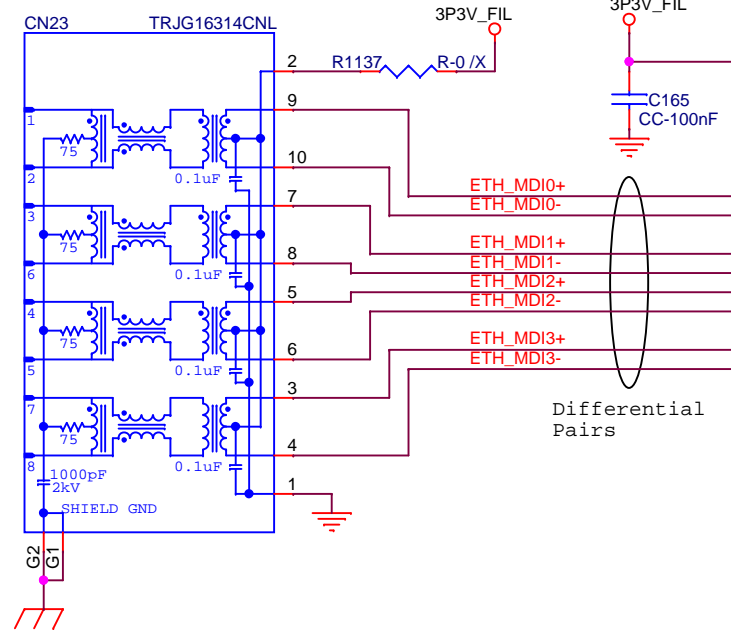
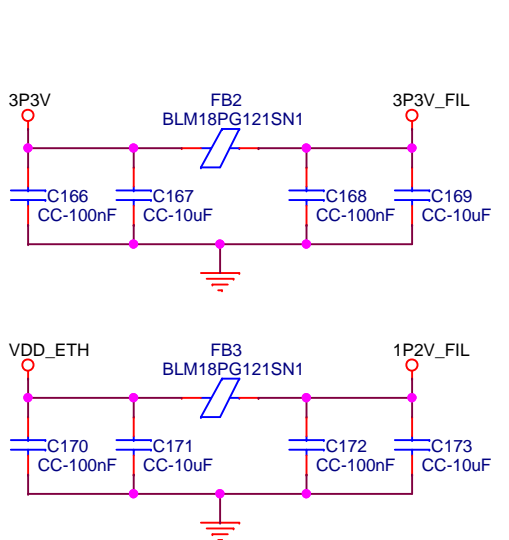
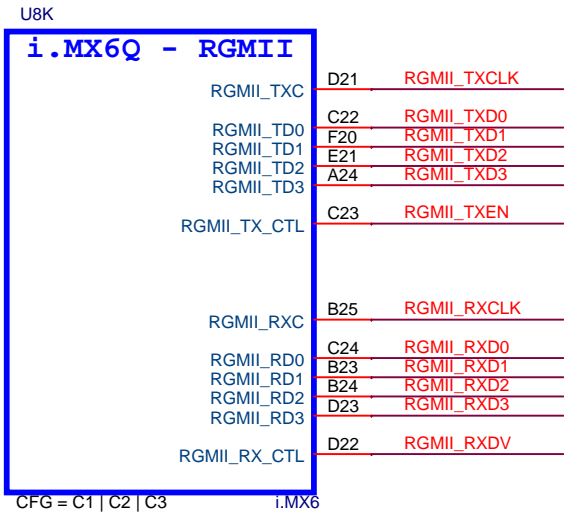
- [7] DRAM\_D32
- [7] DRAM\_D33
- [7] DRAM\_D34
- [7] DRAM\_D35
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- [7] DRAM\_D37
- [7] DRAM\_D38
- [7] DRAM\_D39
- [7] DRAM\_D40
- [7] DRAM\_D41
- [7] DRAM\_D42
- [7] DRAM\_D43
- [7] DRAM\_D44
- [7] DRAM\_D45
- [7] DRAM\_D46
- [7] DRAM\_D47
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- [7] DRAM\_D49
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- [7] DRAM\_D55
- [7] DRAM\_D56
- [7] DRAM\_D57
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- [7] DRAM\_D59
- [7] DRAM\_D60
- [7] DRAM\_D61
- [7] DRAM\_D62
- [7] DRAM\_D63
  
- [7] DRAM\_A0
- [7] DRAM\_A1
- [7] DRAM\_A2
- [7] DRAM\_A3
- [7] DRAM\_A4
- [7] DRAM\_A5
- [7] DRAM\_A6
- [7] DRAM\_A7
- [7] DRAM\_A8
- [7] DRAM\_A9
- [7] DRAM\_A10
- [7] DRAM\_A11
- [7] DRAM\_A12
- [7] DRAM\_A13
- [7] DRAM\_A14
- [7] DRAM\_A15
  
- [7] DRAM\_SDBA0
- [7] DRAM\_SDBA1
- [7] DRAM\_SDBA2
  
- [7] DRAM\_SDQS4
- [7] DRAM\_SDQS4\_B
- [7] DRAM\_DQM4
  
- [7] DRAM\_SDQS5
- [7] DRAM\_SDQS5\_B
- [7] DRAM\_DQM5
  
- [7] DRAM\_SDQS6
- [7] DRAM\_SDQS6\_B
- [7] DRAM\_DQM6
  
- [7] DRAM\_SDQS7
- [7] DRAM\_SDQS7\_B
- [7] DRAM\_DQM7
  
- [7] DRAM\_RAS\_B
- [7] DRAM\_CAS\_B
- [7] DRAM\_WE\_B
  
- [7] DRAM\_CS0\_B
  
- [7] DRAM\_SDCKE0
  
- [7] DRAM\_SDODT0
  
- [7] DRAM\_RESET\_B
  
- [7] DRAM\_SDCLK0
- [7] DRAM\_SDCLK0\_B

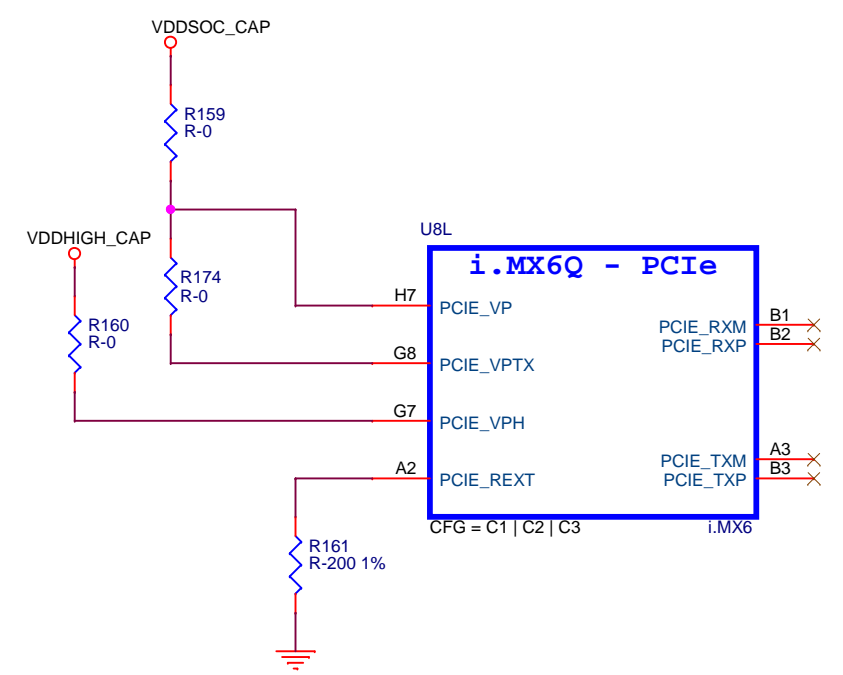
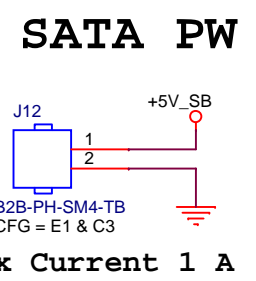
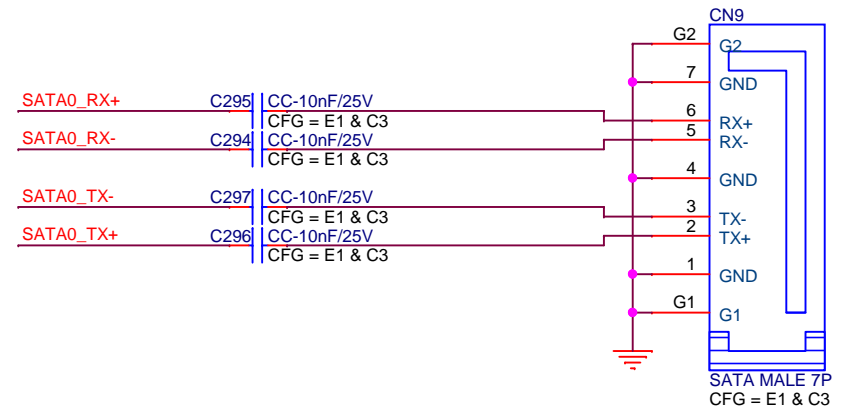
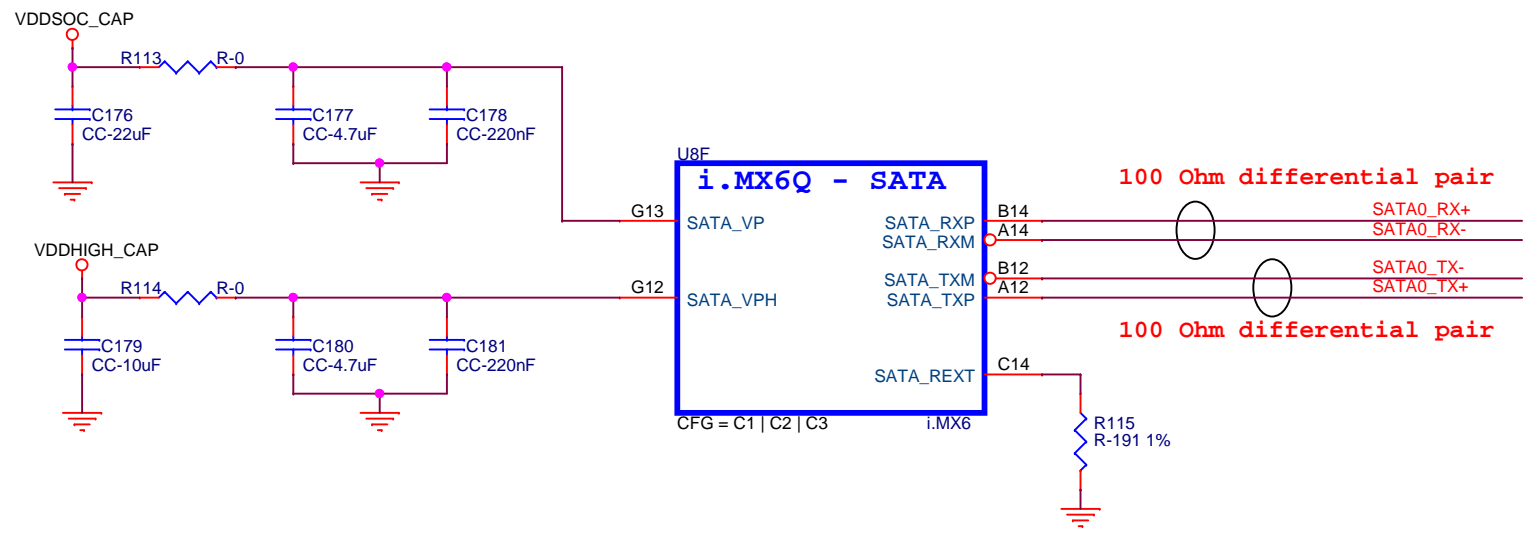


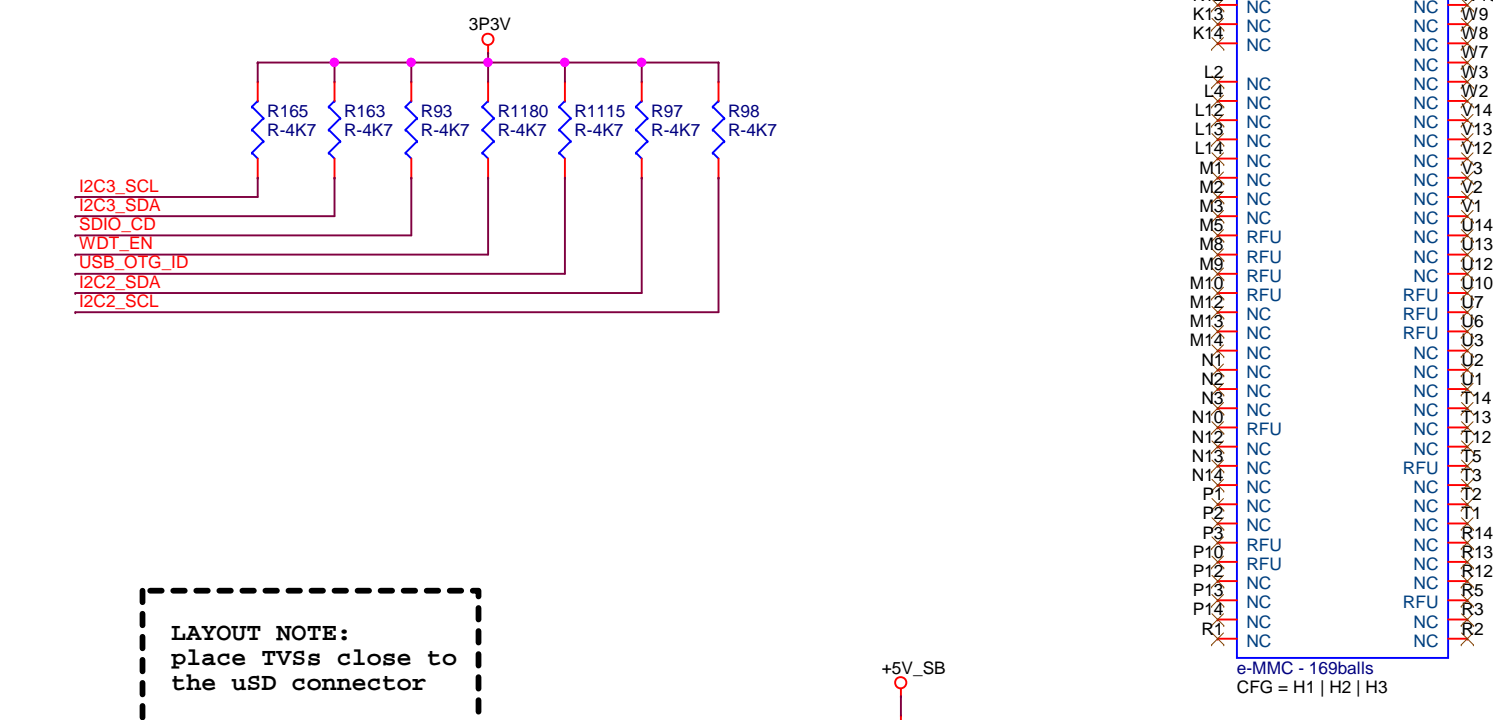
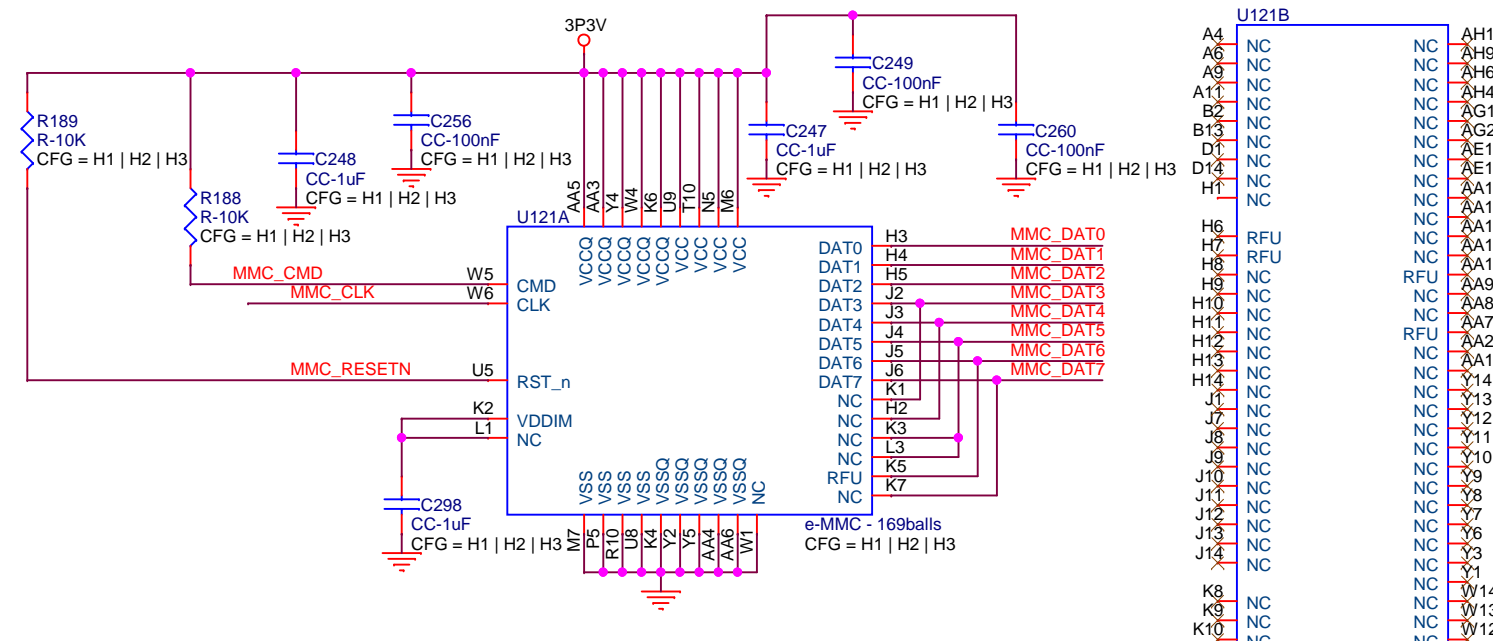
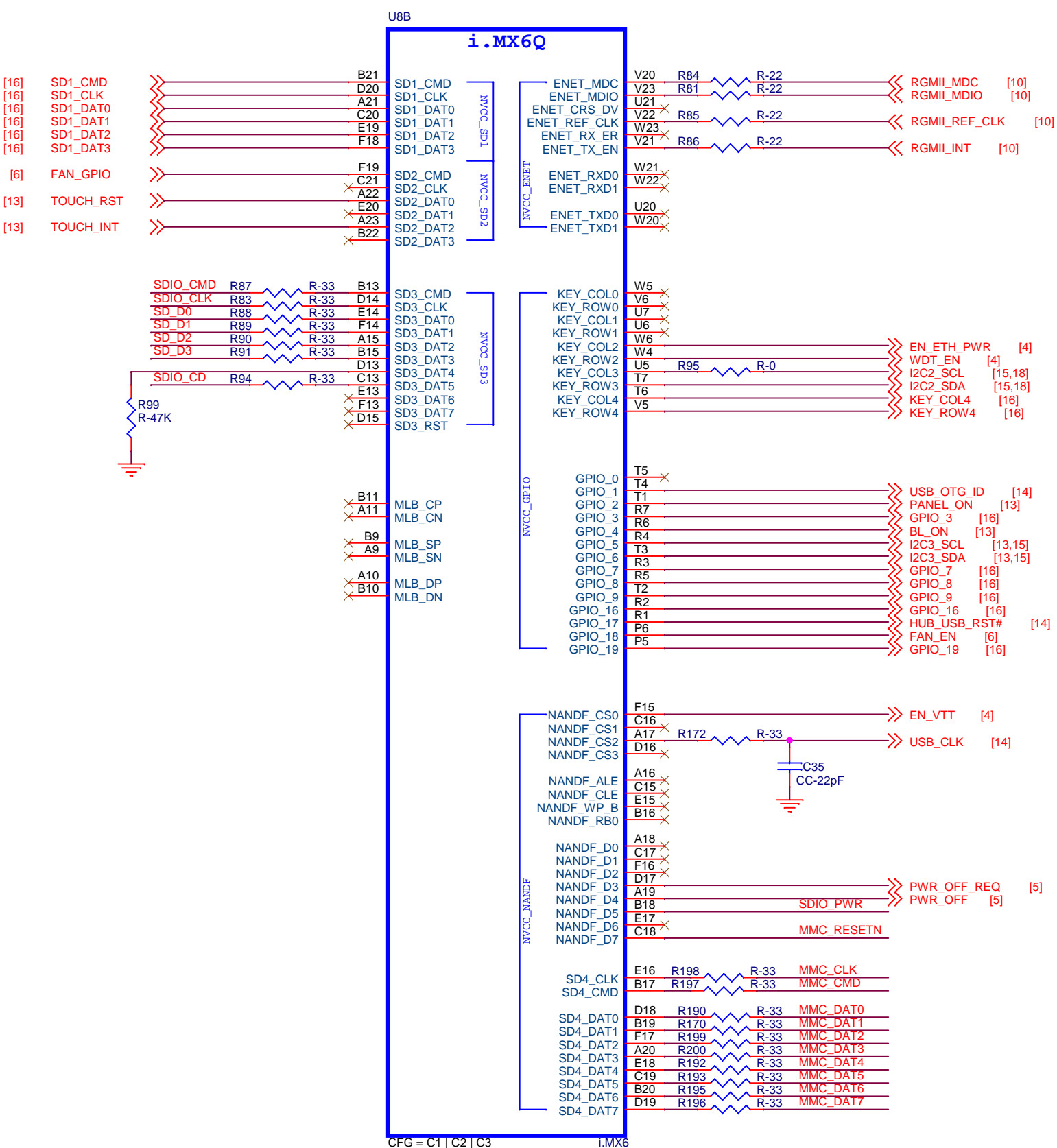




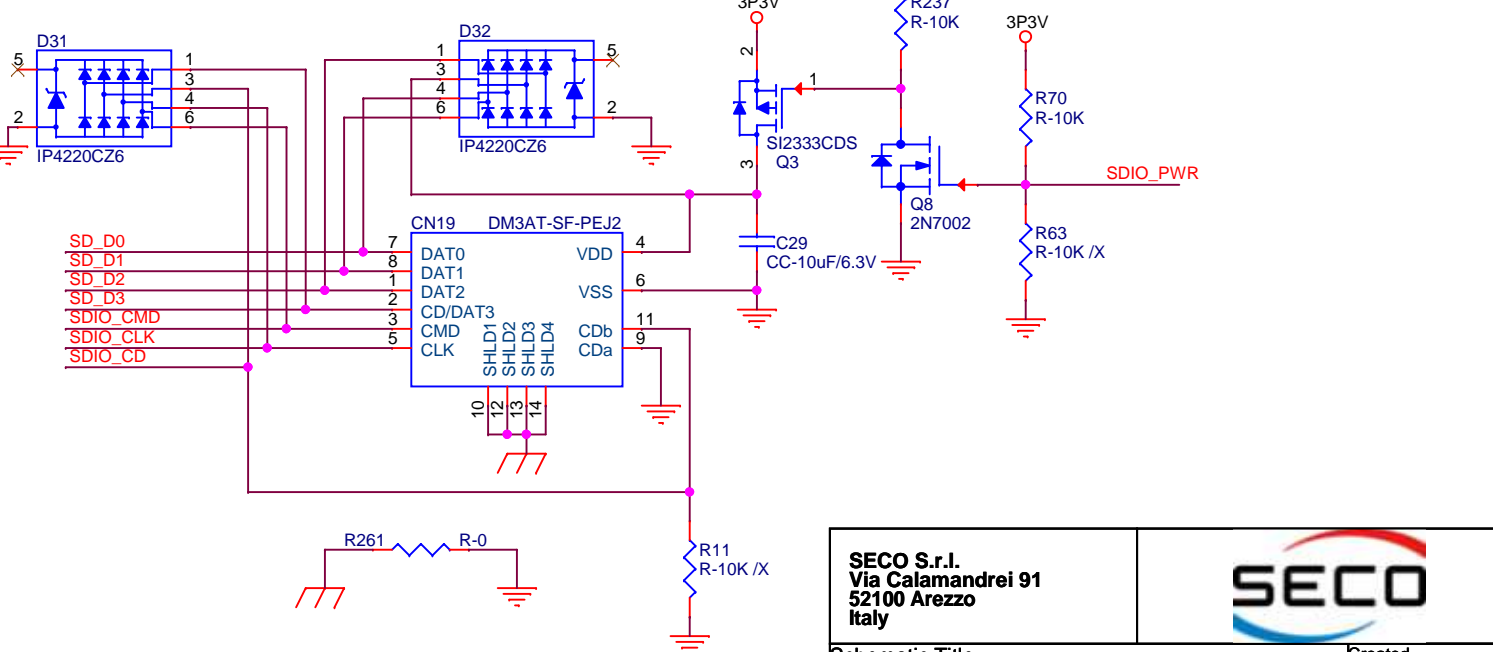
## Debug UART







**LAYOUT NOTE:**  
place TVSSs close to the uSD connector



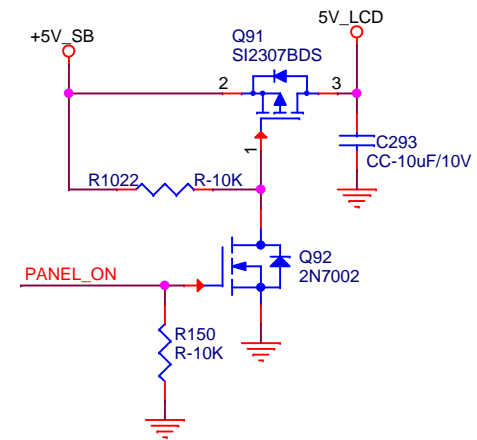
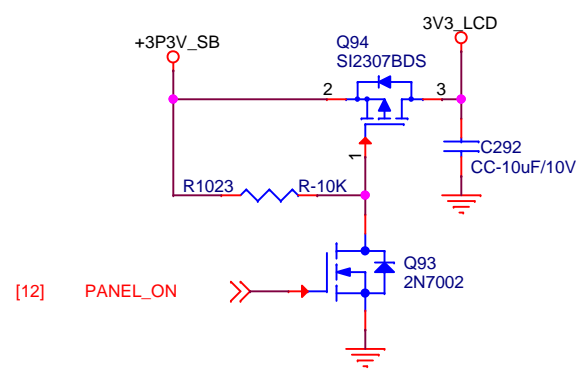
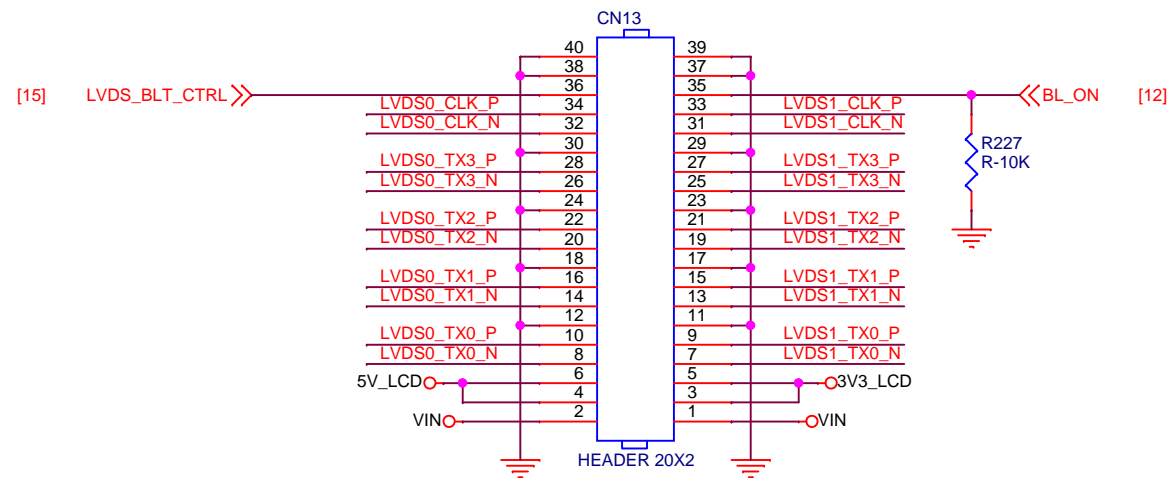
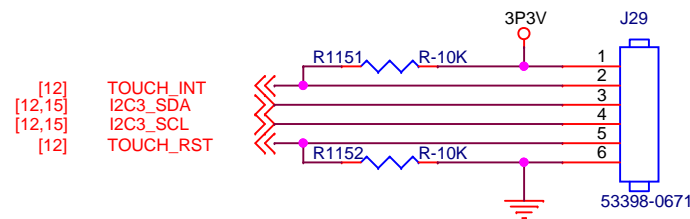
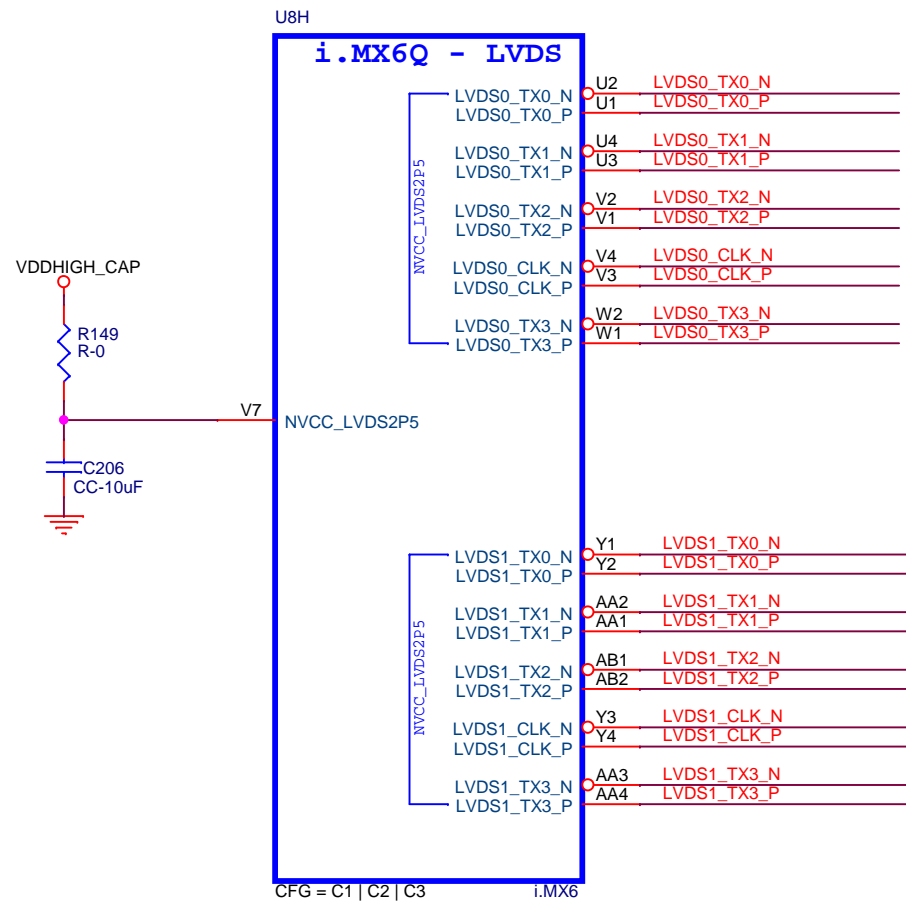
**SECO S.r.l.**  
Via Calamandrei 91  
52100 Arezzo  
Italy

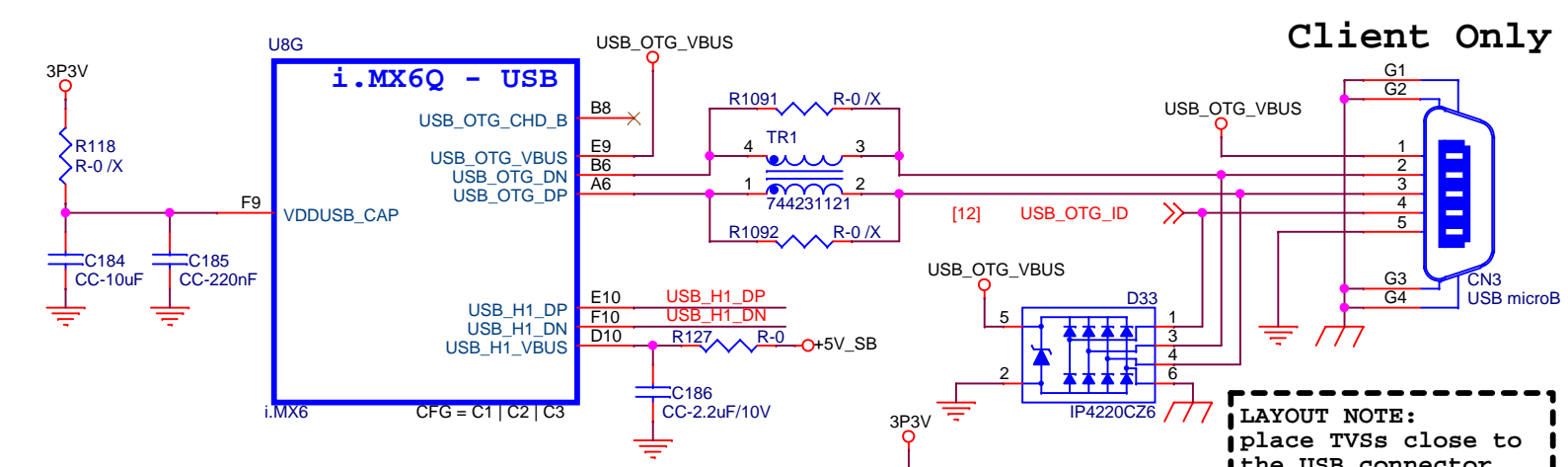
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Schematic Title: **SBC-A62-J** Created: \_\_\_\_\_

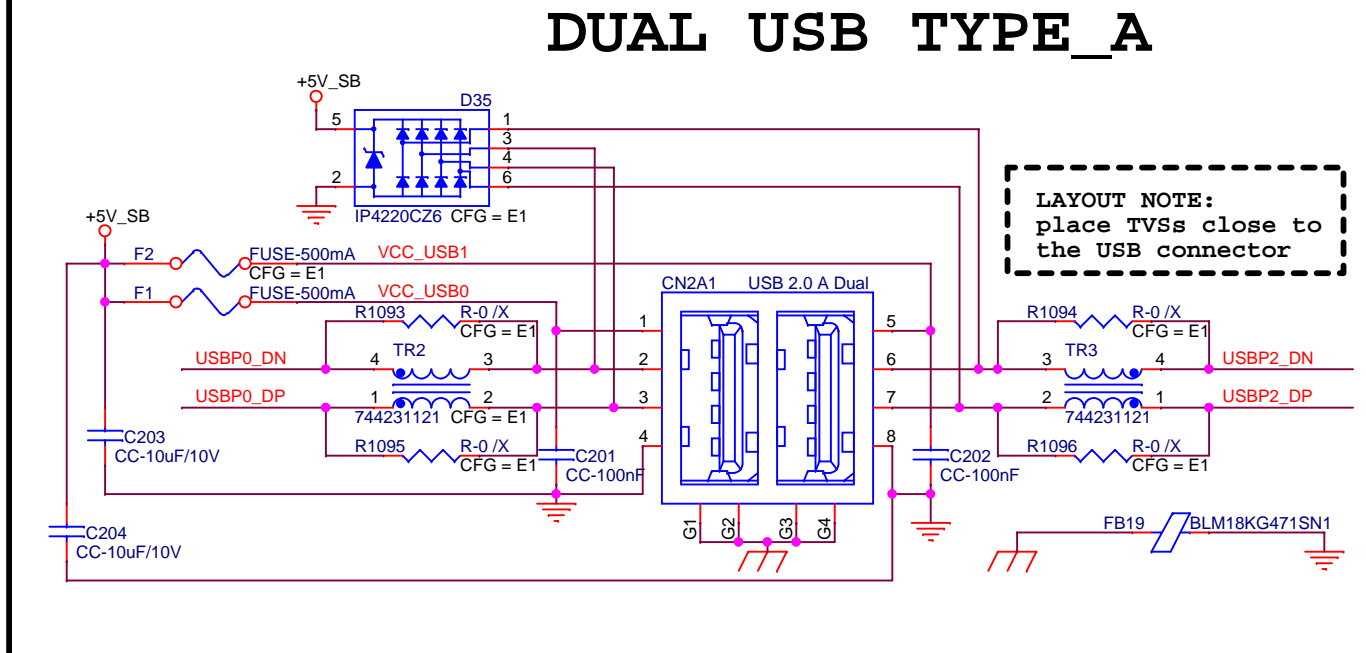
Size: A3 Page Name: SDIO/eMMC Rev: 1

Date: Wednesday, February 17, 2016 Sheet: 12 of 19



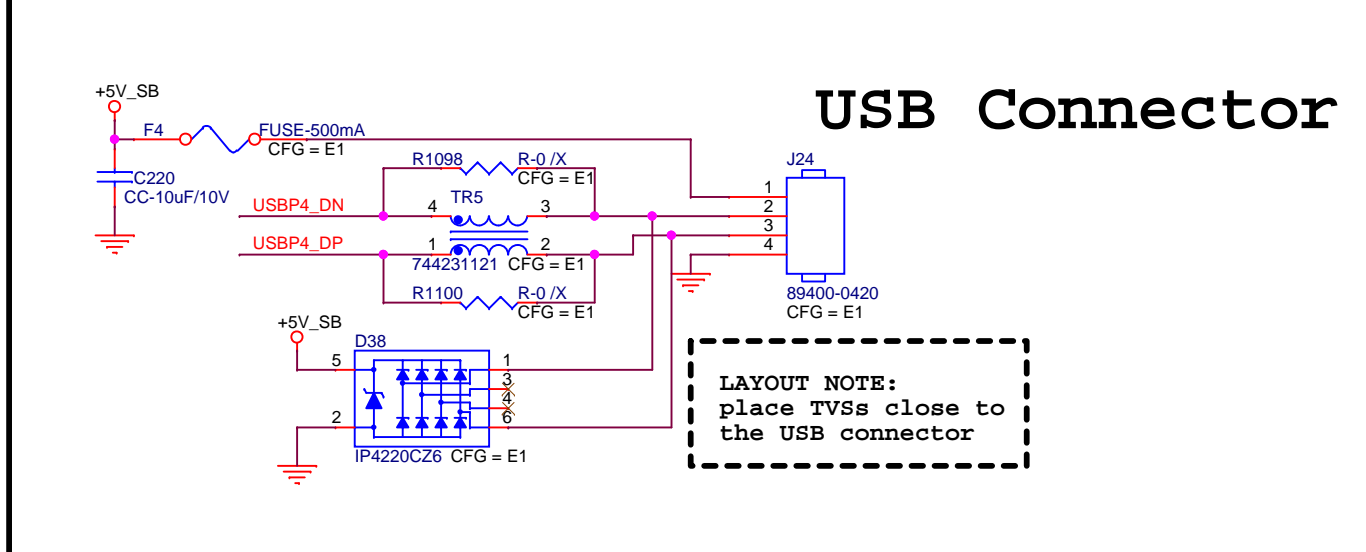
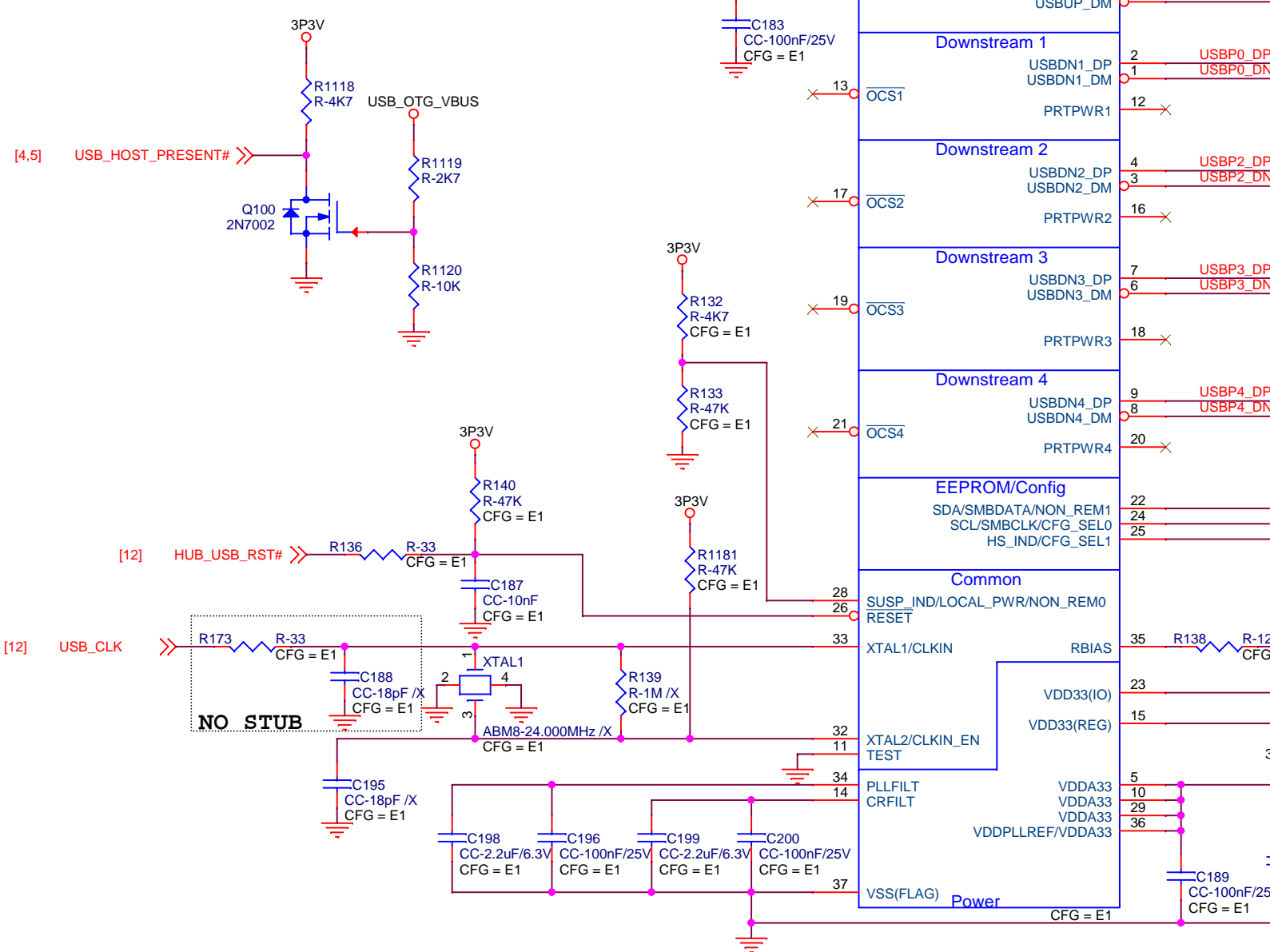


**Client Only**



LAYOUT NOTE:  
place TVSS close to the USB connector

**USB - HOST**



LAYOUT NOTE:  
place TVSS close to the USB connector

NO STUB

USB\_H1\_DP R1116 R-0

CFG = E2

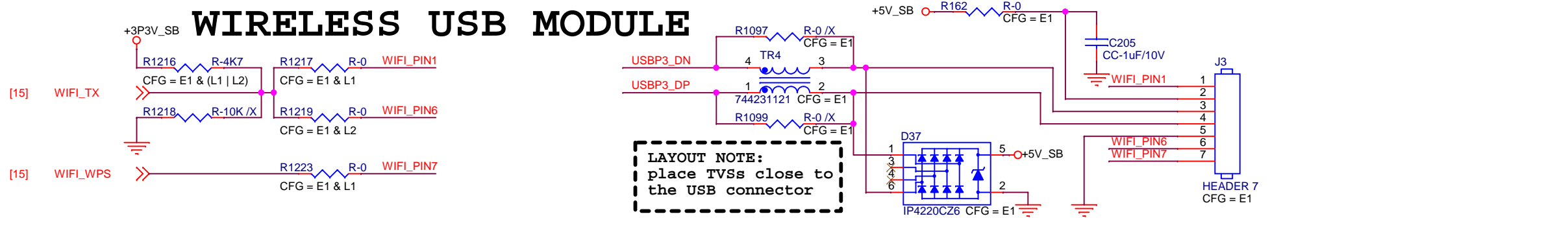
USBP2\_DP R1117 R-0

CFG = E2

USBP2\_DN

NO STUB

**WIRELESS USB MODULE**



LAYOUT NOTE:  
place TVSS close to the USB connector

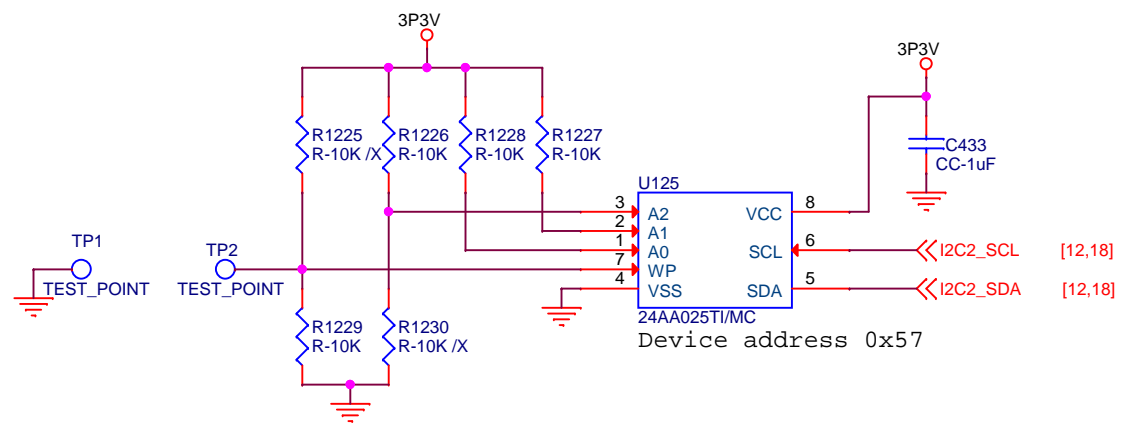
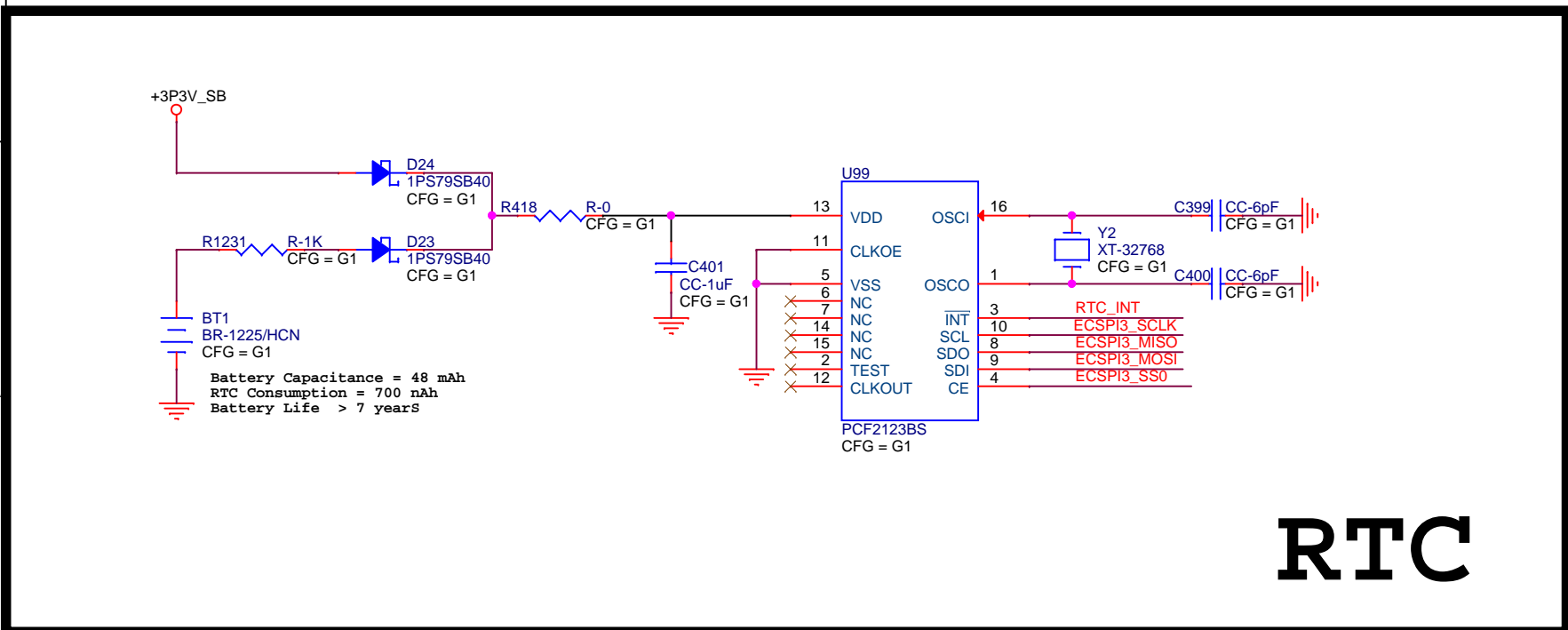
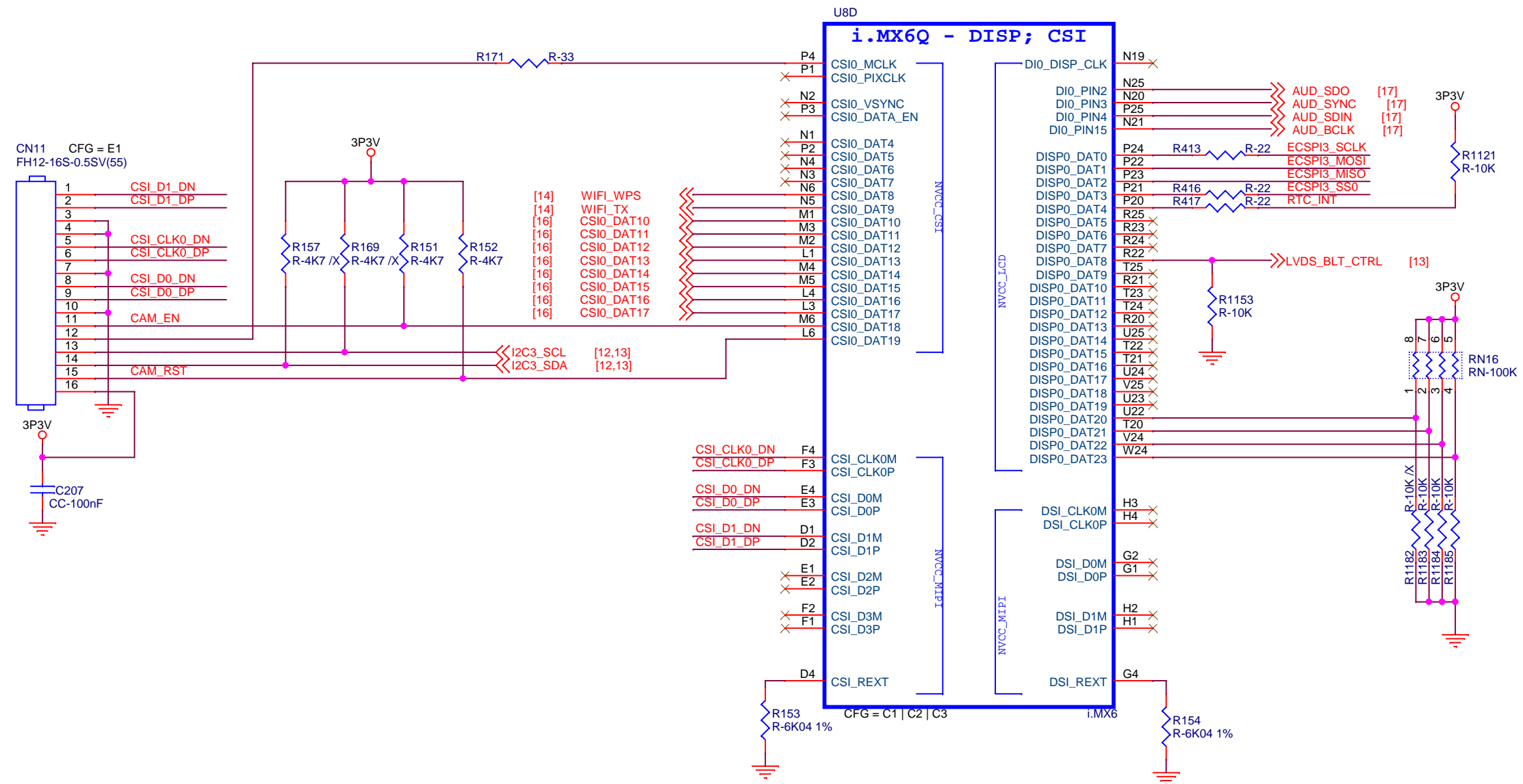
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52100 Arezzo  
Italy

Schematic Title  
**SBC-A62-J**

Created

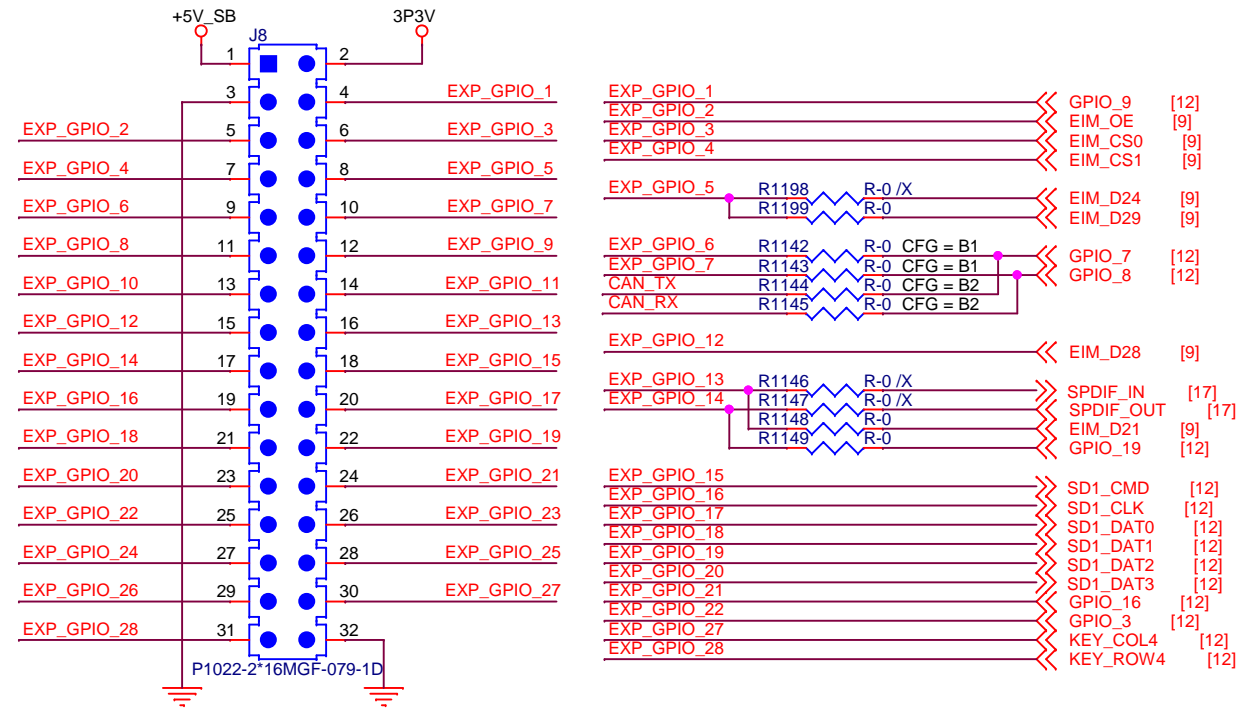
Size A3 Page Name USB Rev 1

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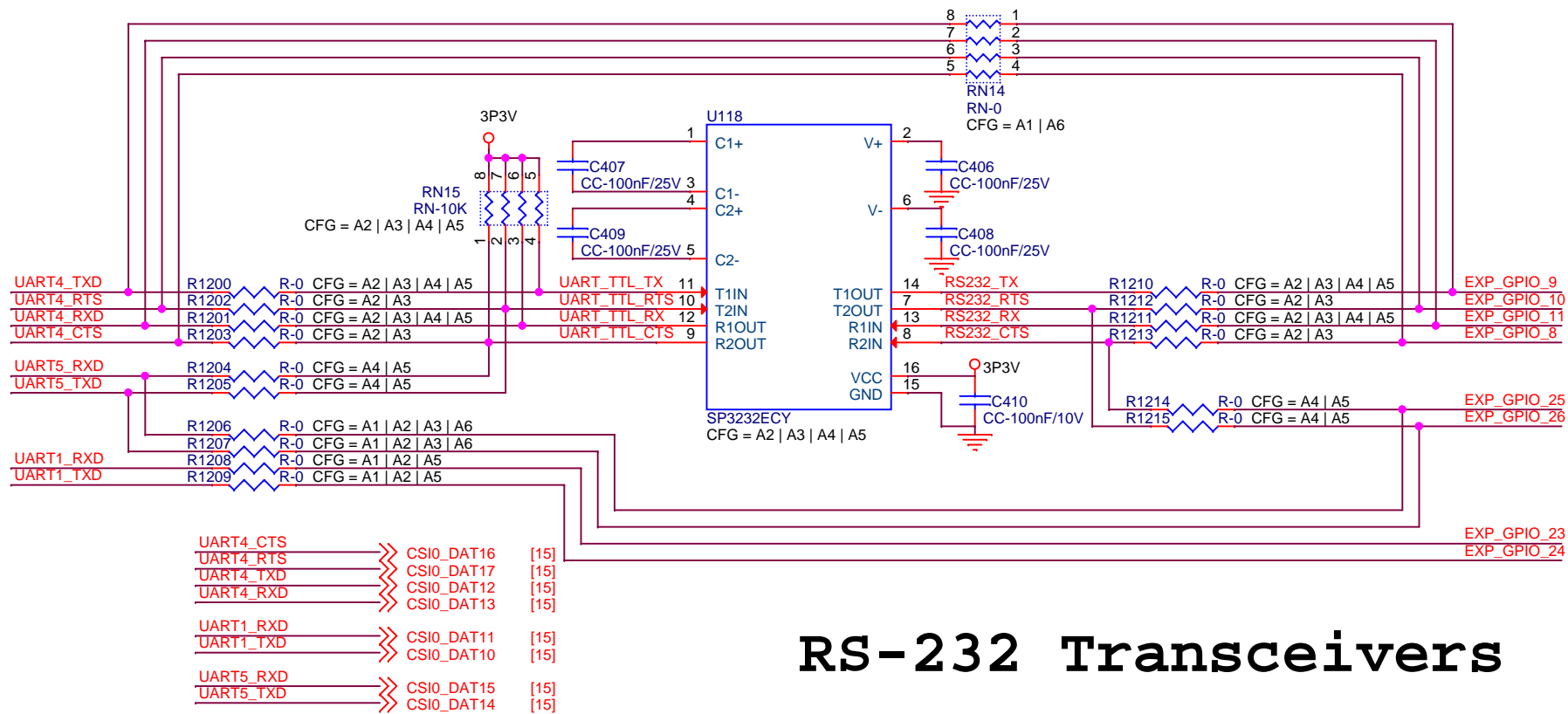
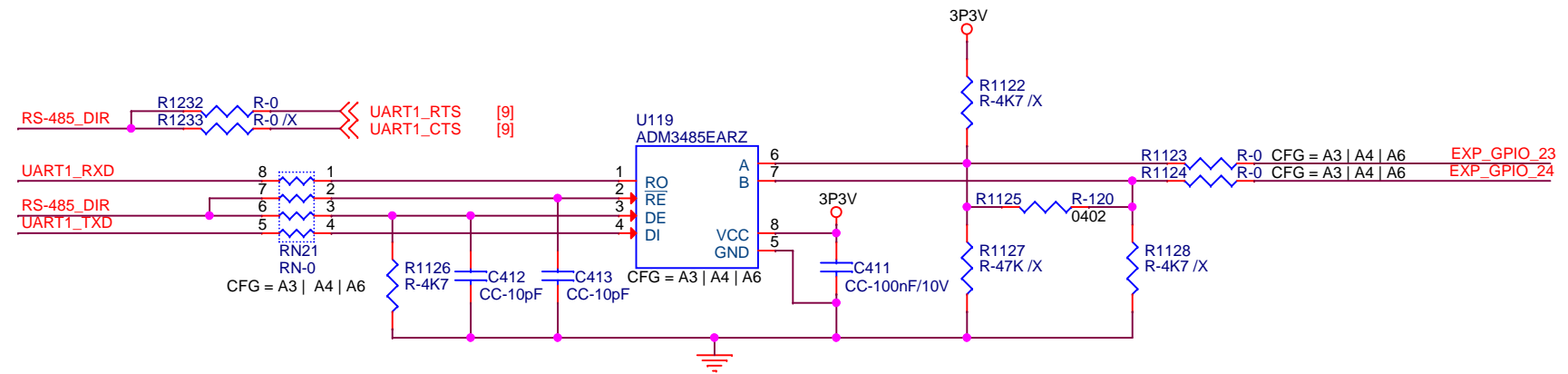
**RTC**

# Expansion Features



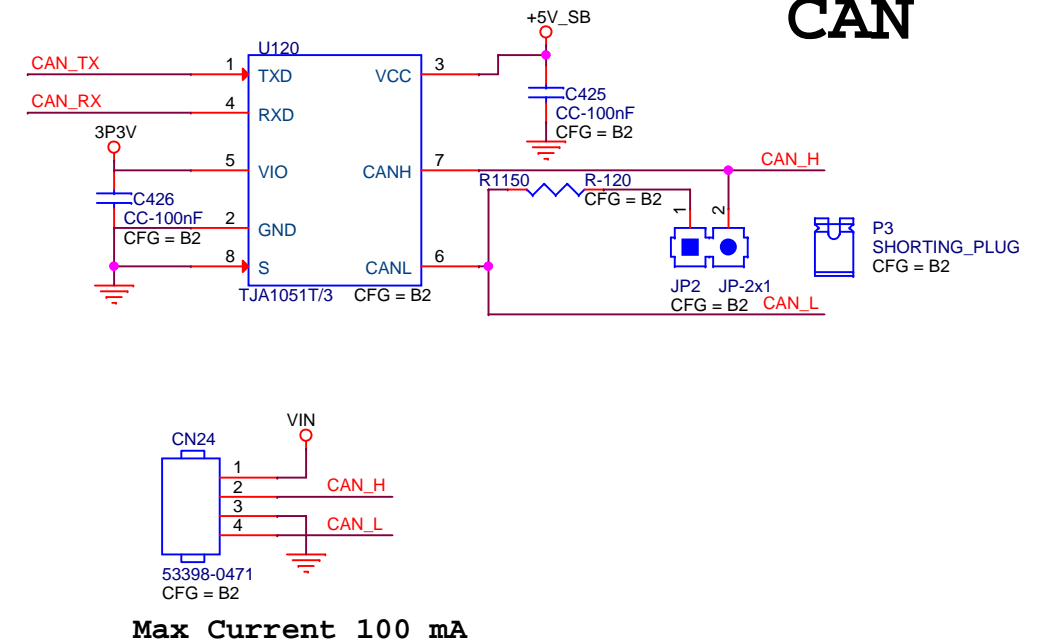
Max Current Pin1 500 mA  
Max Current Pin2 500 mA

# RS-485 Half-Duplex



# RS-232 Transceivers

# CAN



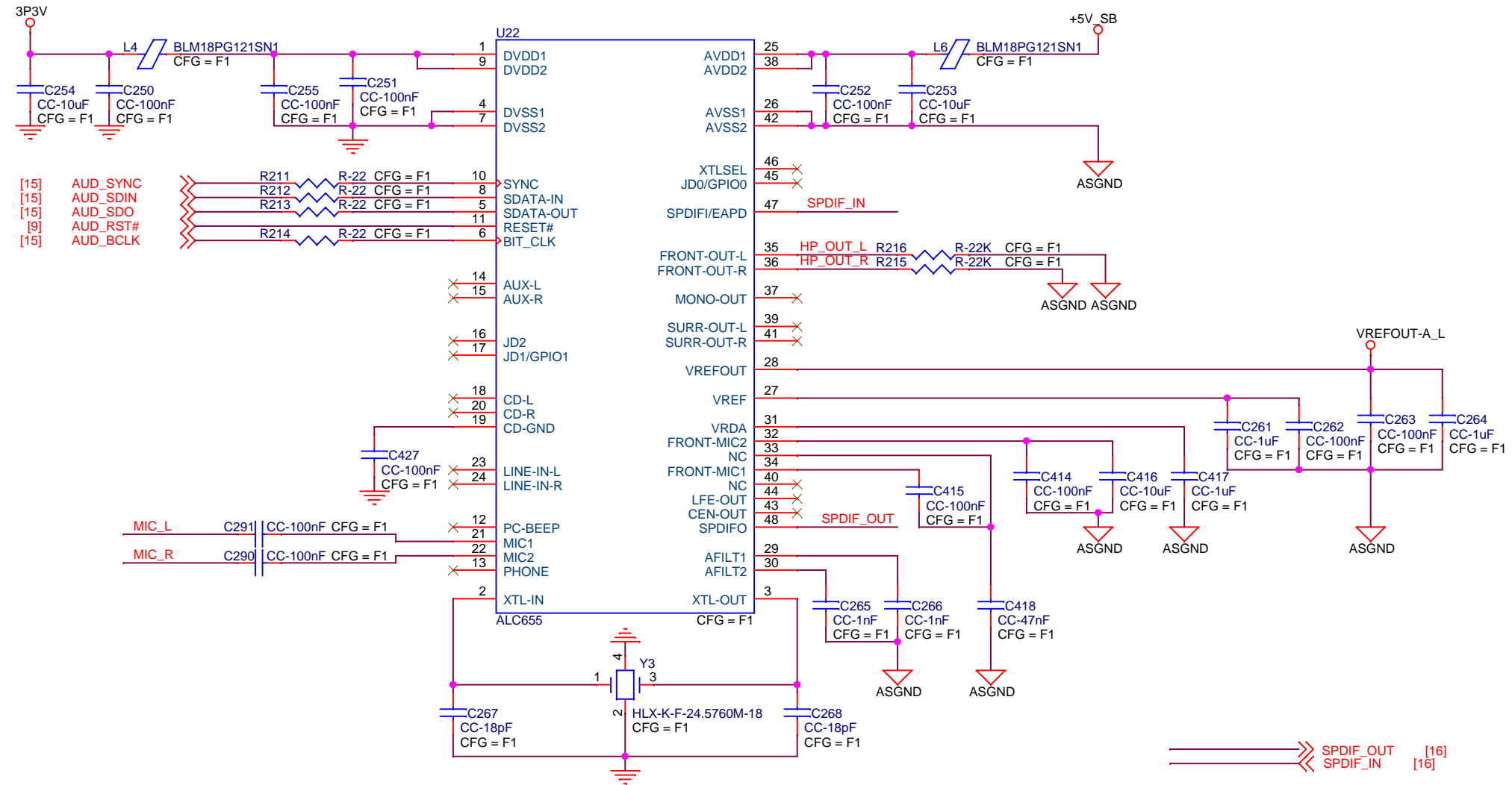
Max Current 100 mA

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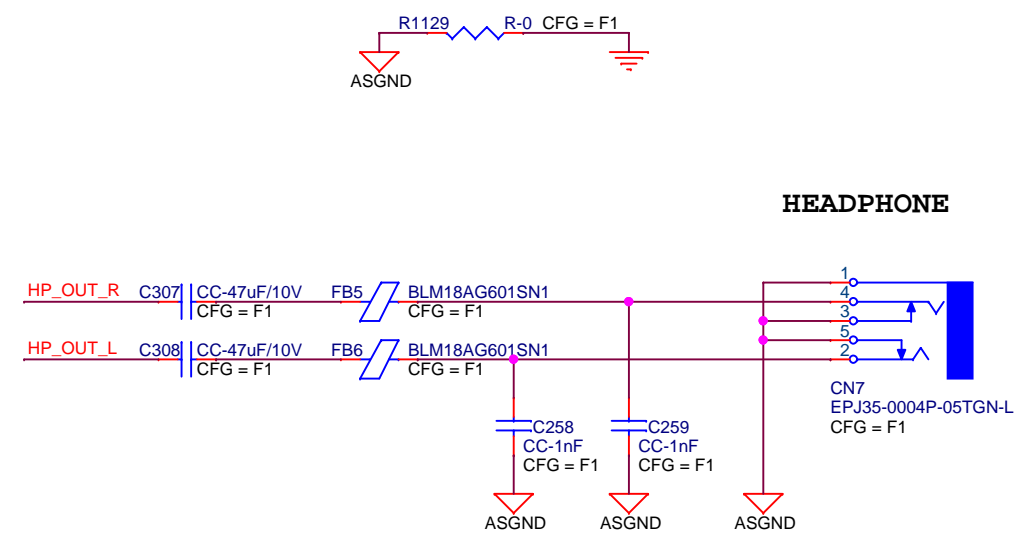
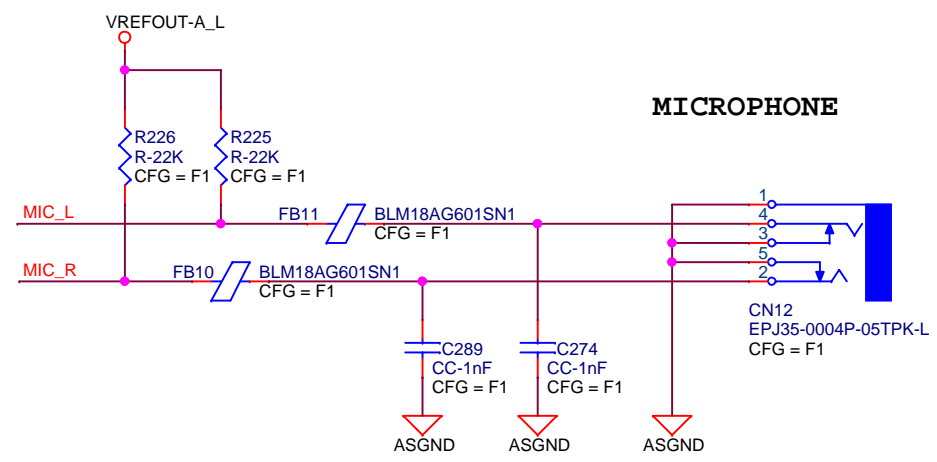


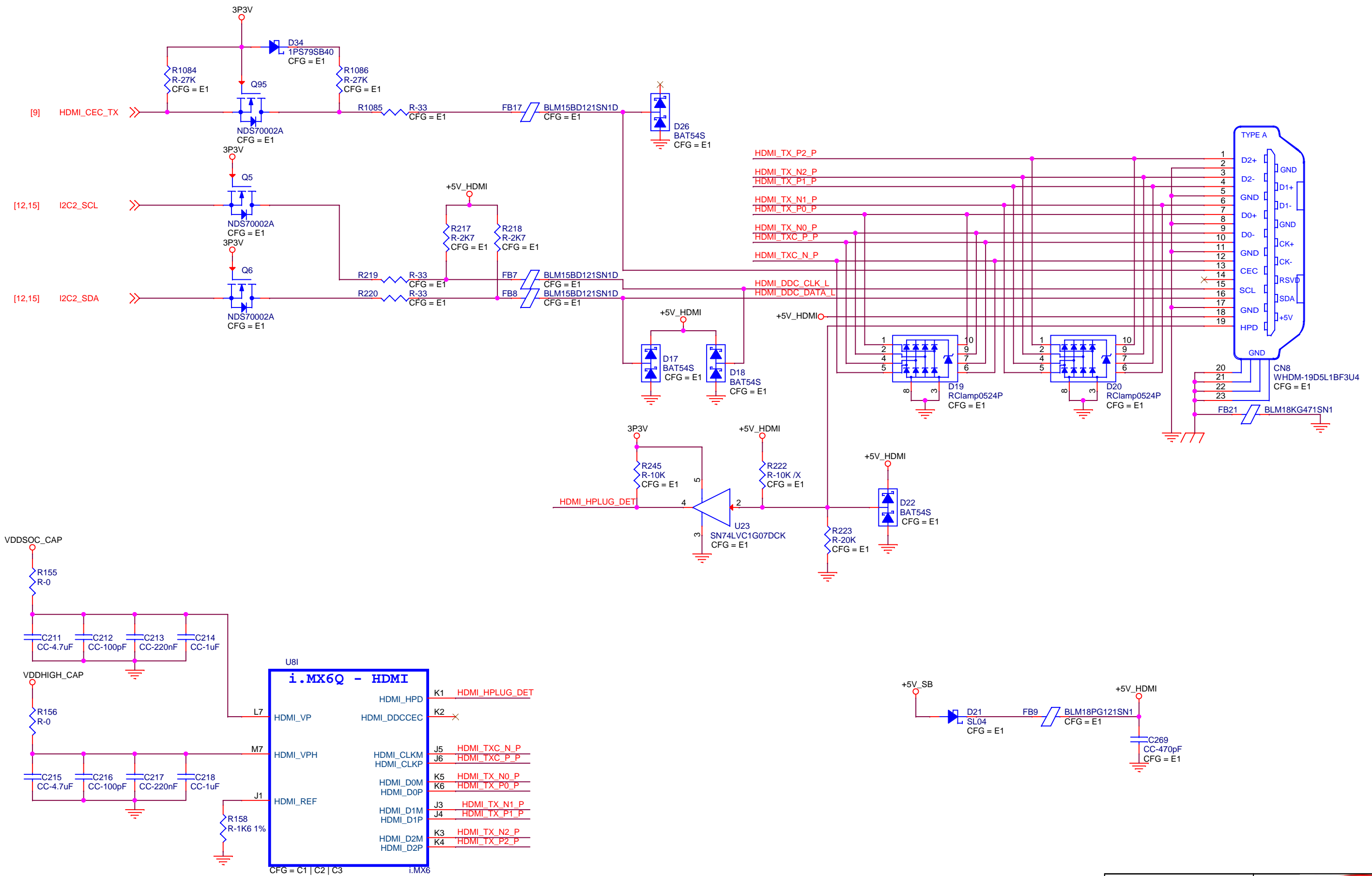
# AC'97 AUDIO CODEC



- [15] AUD\_SYNC
- [15] AUD\_SDIN
- [15] AUD\_SDO
- [9] AUD\_RST#
- [15] AUD\_BCLK

SPDIF\_OUT [16]  
SPDIF\_IN [16]





# Configurations

OPTION NAME	CFG	OPTION DESCRIPTION	NOTE
UART	A1	UART_4 TTL Full /_8 TTL tx,rx /_9 TTL Full	
	A2	UART_4 RS-232 Full /_8 TTL tx,rx /_9 TTL Full	
	A3	UART_4 RS-232 Full /_8 RS-485 /_9 TTL Full	
	A4	UART_4 RS-232 tx,rx /_8 RS-485 /_9 RS-232 tx,rx	
	A5	UART_4 RS-232 tx,rx /_8 TTL tx,rx /_9 RS-232 tx,rx	
	A6	UART_4 TTL Full /_8 RS-485 /_9 TTL Full	
CAN	B1	TTL CAN Bus signals on expansion connector	
	B2	CAN Bus signals on dedicated connector	
PROCESSOR	C1	iMX6_SOLO	P/N i.MX6S
	C2	iMX6_DUAL_LITE	P/N i.MX6DL
	C3	iMX6_QUAD_CORE	P/N i.MX6Q
RAM	D1	512 MB 32 bit	Memory chips used: P/N MT41K128M16JT-125:K
	D2	1 GB 64 bit	Memory chips used: P/N MT41K128M16JT-125:K
	D3	2 GB 64 bit	Memory chips used: P/N MT41K256M16HA-125:E
FULL	E1	Configuration: Full	
	E2	Configuration: Minimal	
AUDIO	F1	AC'97 Codec + Audio Jack	
RTC	G1	RTC Low Power	
	G2	RTC iMX6 with external battery	
eMMC	H1	eMMC 4GB	
	H2	eMMC 8GB	
	H3	eMMC 16GB	
Wi-Fi Module	L1	7 pin GWF-3M08 module's pinout	
	L2	6 pin GWF-M05 module's pinout	

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**SBC-A62-J**

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Size A3 Page Name  
**CONFIGURATIONS**

Rev  
**1**

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