# SMARC®

## User Manual

## SOM-SMARC-MX8M-PLUS

SMARC® Rel. 2.1.1 compliant module with NXP i.MX 8M Plus Applications Processors



**SMARC** module

**SGeT** STANDARDIZATION GROUP FOR EMBEDDED TECHNOLOGIES

**SECO**

# REVISION HISTORY

| Revision | Date | Note | Rif |
|---|---|---|---|
| 1.0 | 8th February 2022 | First official release | SO |
| 1.1 | 23rd February 2022 | Minor corrections<br>SoC to SMARC® pinout | SO |
| 1.2 | 27th September 2022 | Updated SDIO electrical level for SDR104 | SO |
| 1.3 | 4th March 2024 | Updated to new commercial name. New manual layout. References updated.<br>Typo corrected on signals' names on pins S17, S18, S84, S87, S90<br>USB5_EN_OC# signal description added<br>QSPI_CS1# signal added | SB |
| | | | |

# INDEX

# Chapter 1.
## INTRODUCTION

- Warranty
- Information and assistance
- RMA number request
- Safety
- Electrostatic Discharges
- RoHS compliance
- Terminology and definitions
- Reference specifications

# 1.1   Warranty

This product is subject to the Italian Law Decree 24/2002, acting European Directive 1999/44/CE on matters of sale and warranties to consumers.

The warranty on this product lasts for 1 year.

Under the warranty period, the Supplier guarantees the buyer assistance and service for repairing, replacing or credit of the item, at the Supplier's own discretion.

Shipping costs that apply to non-conforming items or items that need replacement are to be paid by the customer.

Items cannot be returned unless previously authorised by the supplier.

The authorisation is released after completing the specific form available on the web-site https://www.seco.com/us/support/online-rma.html (RMA Online). The RMA authorisation number must be put both on the packaging and on the documents shipped with the items, which must include all the accessories in their original packaging, with no signs of damage to, or tampering with, any returned item.

The error analysis form identifying the fault type must be completed by the customer and has must accompany the returned item.

If any of the above-mentioned requirements for RMA is not satisfied, the item will be shipped back and the customer will have to pay any and all shipping costs.

Following a technical analysis, the supplier will verify if all the requirements, for which a warranty service applies, are met. If the warranty cannot be applied, the Supplier will calculate the minimum cost of this initial analysis on the item and the repair costs. Costs for replaced components will be calculated separately.

> ⚠️ **Warning!**
> All changes or modifications to the equipment not explicitly approved by SECO S.p.A. could impair the equipment's functionality and could void the warranty

## 1.2 Information and assistance

**What do I have to do if the product is faulty?**

SECO S.p.A. offers the following services:

- SECO website: visit http://www.seco.com to receive the latest information on the product. In most of the cases it is possible to find useful information to solve the problem.
- SECO Sales Representative: the Sales Rep can help to determine the exact cause of the problem and search for the best solution.
- SECO Help-Desk: contact SECO Technical Assistance.  A technician is at disposal to understand the exact origin of the problem and suggest the correct solution.

    E-mail: technical.service@seco.com

    Fax (+39) 0575 350210

- Repair center: it is possible to send the faulty product to the SECO Repair Centre. In this case, follow this procedure:
  - Returned items must be accompanied by a RMA Number. Items sent without the RMA number will be not accepted.
  - Returned items must be shipped in an appropriate package. SECO is not responsible for damages caused by accidental drop, improper usage, or customer neglect.

**Note: Please have the following information before asking for technical assistance:**

- Name and serial number of the product;
- Description of Customer's peripheral connections;
- Description of Customer's software (operating system, version, application software, etc.);
- A complete description of the problem;
- The exact words of every kind of error message encountered.

## 1.3 RMA number request

To request an RMA number, please visit SECO's web-site. On the home page, please select "RMA Online" and follow the procedure described.

An RMA Number will be sent within 1 working day (only for on-line RMA requests).

## 1.4  Safety

The SOM-SMARC-MX8M-PLUS module uses only extremely low voltages.

While handling the board, please use extreme caution to avoid any kind of risk or damages to electronic components.

> **!** Always switch the power off, unplug the power supply unit and wait until the unit has cooled down, before handling the board and/or connecting cables or other boards.
>
> Avoid using metallic components - like paper clips, screws and similar - near the board when connected to a power supply, to avoid short circuits due to unwanted contacts with other board components.
>
> If the board has become wet, never connect it to any external power supply unit or battery.

## 1.5  Electrostatic Discharges

The SOM-SMARC-MX8M-PLUS module, like any other electronic product, is an electrostatic sensitive device: high voltages caused by static electricity could damage some or all the devices and/or components on-board.

> **!** Whenever handling any of these boards, ground yourself through an anti-static wrist strap. Placement of the board on an anti-static surface is also highly recommended.

## 1.6  RoHS compliance

The SOM-SMARC-MX8M-PLUS module is designed using RoHS compliant components and is manufactured on a lead-free production line. It is therefore fully RoHS compliant.

# 1.7 Safety Policy

In order to meet the safety requirements of IEC 62368-1:2018 standard for Audio/Video, information and communication technology equipment, the SOM-SMARC-MX8M-PLUS Module shall be:

- used exclusively on SMARC 2.1 fully compliant Carrier boards;

- connections from or to the Module have to be compliant to ES1 requirements;

- used inside a fire enclosure made of non-combustible material or V-1 material (the fire enclosure is not necessary if the maximum power supplied to the module never exceeds 100 W, even in worst-case fault);

- used along with CPU Heatspreader/heatsinks designed according to the thermal characteristics indicated in the par. 2.2 and to the mechanical characteristics indicated in par.2.4.

The manufacturer which includes a SOM-SMARC-MX8M-PLUS module in his end-user product shall:

- Install the device inside an enclosure compliant with all applicable IEC 62368-1 requirements;

- Prevent children from accessing the board;

- Prescribe temperature and humidity range for operating, transport and storage conditions;

- verify the compliance with B.2 and B.3 clauses of the IEC 62368-1 standard when the module works in its own final operating condition;

- provide an instructional safeguard against thermal injuries, according to clause 9.5.2 of the above mentioned standard. This instructional safeguard must be placed both on end-user product's User Manual and on the products itself (Danger Label IEC 60417-5041, it must be placed near the CPU or its heatsink);

- When an heatsink with FAN is used, then the FAN should be managed with signals made available by SMARC Card Edge Connector of the SOM-SMARC-MX8M-PLUS module. Its electrical characteristics must be compliant to the requirements of SMARC Rel.2.1 standard.

# 1.8 Terminology and definitions

| | |
|---|---|
| API | Application Program Interface, a set of commands and functions that can be used by programmers for writing software for specific Operating Systems |
| BTLE | Bluetooth Low Energy, a wireless personal area network technology |
| CAN Bus | Controller Area network, a protocol designed for in-vehicle communication |
| CSI2 | MIPI Camera Serial Interface, 2nd generation standard regulating communication between a peripheral device (camera) and a host processor |
| DDC | Display Data Channel, a kind of I2C interface for digital communication between displays and graphics processing units (GPU) |
| DDR | Double Data Rate, a typology of memory devices which transfer data both on the rising and on the falling edge of the clock. |
| DVI | Digital Visual interface, a type of display video interface |
| FFC/FPC | Flexible Flat Cable / Flat Panel Cable |
| GBE | Gigabit Ethernet |
| Gbps | Gigabits per second |
| GND | Ground |
| GPI/O | General purpose Input/Output |
| HDMI | High Definition Multimedia Interface, a digital audio and video interface |
| I2C Bus | Inter-Integrated Circuit Bus, a simple serial bus consisting only of data and clock line, with multi-master capability |
| I2S | Inter-Integrated Circuit Sound, an audio serial bus protocol interface developed by Philips (now NXP) in 1986 |
| LPDDR4 | Low-Power Double Data Rate Synchronous Dynamic Random Access Memory, $4^{th}$ generation |
| LVDS | Low Voltage Differential Signalling, a standard for transferring data at very high speed using inexpensive twisted pair copper cables, usually used for video applications |
| Mbps | Megabits per second |
| MIPI | Mobile Industry Processor Interface alliance |
| MMC/eMMC | MultiMedia Card / embedded MMC, a type of memory card, having the same interface as the SD card. The eMMC is the embedded version of the MMC. They are devices that incorporate the flash memories on a single BGA chip. |
| N.A. | Not Applicable |
| N.C. | Not Connected |
| OpenGL | Open Graphics Library, an Open Source API dedicated to 2D and 3D graphics |
| OpenVG | Open Vector Graphics, an Open Source API dedicated to hardware accelerated 2D vector graphics |

| | |
|---|---|
| OTG | On-the-Go, a specification that allows to USB devices to act indifferently as Host or as a Client, depending on the device connected to the port. |
| PCI-e | Peripheral Component Interface Express |
| PWM | Pulse Width Modulation |
| PWR | Power |
| RGMII | Reduced Gigabit Reduced Media Independent Interface, a standard interface between the Ethernet Media Access Control (MAC) and the Physical Layer (PHY) |
| SD | Secure Digital, a memory card type |
| SDIO | Secure Digital Input/Output, an evolution of the SD standard that allows the use of the same SD interface to drive different Input/Output devices, like cameras, GPS, Tuners and so on. |
| SM Bus | System Management Bus, a subset of the I2C bus dedicated to communication with devices for system management, like a smart battery and other power supply-related devices. |
| SPI | Serial Peripheral Interface, a 4-Wire synchronous full-duplex serial interface which is composed of a master and one or more slaves, individually enabled through a Chip Select line. |
| TBM | To be measured |
| TMDS | Transition-Minimized Differential Signalling, a method for transmitting high speed serial data, normally used on DVI and HDMI interfaces |
| TTL | Transistor-transistor Logic |
| USB | Universal Serial Bus |
| uSDHC | Ultra Secure Digital Host Controller |

# 1.9 Reference specifications

Here below it is a list of applicable industry specifications and reference documents.

| Reference | Link |
|---|---|
| CAN Bus | https://www.iso.org/standard/63648.html |
| CSI | https://www.mipi.org/specifications/csi-2 |
| DDC | http://www.vesa.org |
| Gigabit Ethernet | https://www.ieee802.org/3/ |
| HDMI | http://www.hdmi.org |
| I2C | https://www.nxp.com/docs/en/user-guide/UM10204.pdf |
| I2S | https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf |
| LVDS | http://www.ti.com/ww/en/analog/interface/lvds.shtml and http://www.ti.com/lit/ml/snla187/snla187.pdf |
| MIPI | http://www.mipi.org |
| MMC/eMMC | http://www.jedec.org/committees/jc-64 |
| NXP i.MX 8M Plus processor | i.MX 8M Plus | Cortex-A53/M7 | NXP Semiconductors |
| OpenGL | http://www.opengl.org |
| OpenVG | http://www.khronos.org/openvg |
| PCI Express | http://www.pcisig.com/specifications/pciexpress |
| SMARC Design Guide 2.1.1 | https://sget.org/wp-content/uploads/2021/05/SMARCmodule_DG_V211.pdf |
| SMARC Hardware Specification 2.1.1 | https://sget.org/wp-content/uploads/2020/05/SMARC_V211.pdf |
| SD Card Association | https://www.sdcard.org/home |
| SDIO | https://www.sdcard.org/developers/overview/sdio |
| SM Bus | http://smbus.org/specs |
| USB 2.0 and USB OTG | https://www.usb.org/document-library/usb-20-specification |
| USB 3.x | https://www.usb.org/sites/default/files/usb_32_202206_0.zip |

# Chapter 2.
# OVERVIEW

- Introduction
- Technical Specifications
- Electrical Specifications
- Mechanical Specifications
- Supported Operating Systems
- Block Diagram
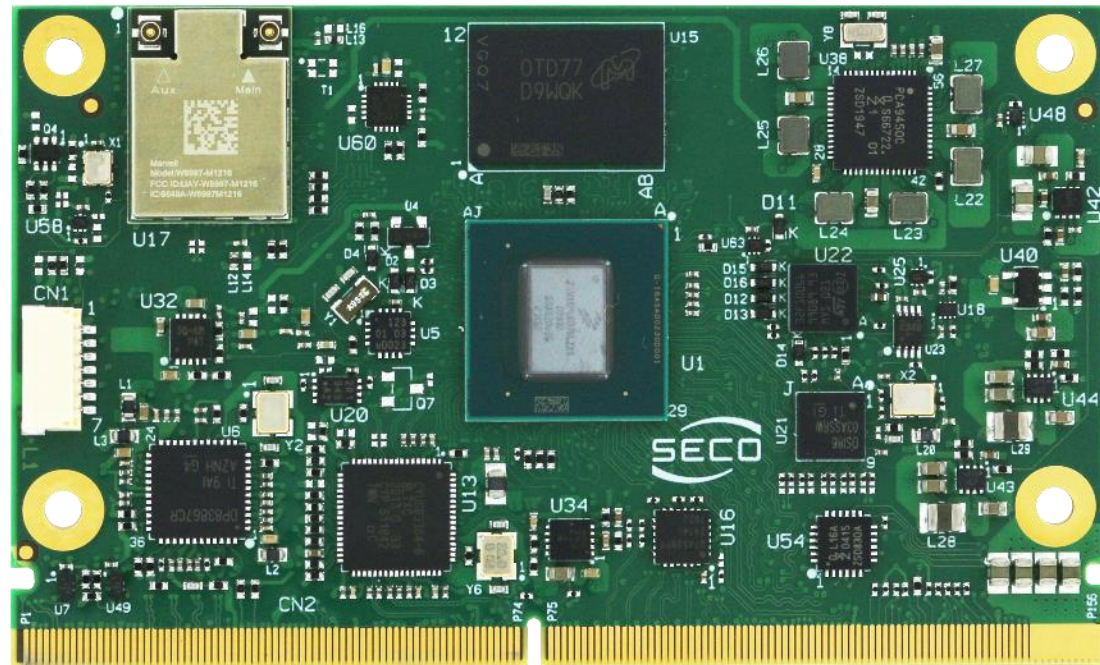
## 2.1 Introduction

SOM-SMARC-MX8M-PLUS is a SMARC Rel. 2.1 compliant module with NXP i.MX 8M Plus family Applications Processors. Featuring multicore and real-time processing together with neural networks acceleration and a vision system. It is a scalable solution designed by SECO for home automation, transportation, digital signage and vending machines, and applicable to scenarios requiring advanced security, connectivity, multimedia and real-time response.

The module offers a very high level of integration, both for all most common used peripherals in the ARM domain and for bus interfaces typically used in the x86 domain, like PCI-Express

Presented in the SMARC ("Smart Mobility ARchitecture") form factor, offering the computing abilities of a standard board, with the possibilities of combining with a ready-to-use carrier board like the SECO CSM-B79 or customised carrier board.

For external interfacing to standard devices, a carrier board with a 314-pin MXM connector is needed. This board will implement all the routing of the interface signals to external standard connectors, as well as the integration of other peripherals/devices not already included in SOM-SMARC-MX8M-PLUS module.

# 2.2 Technical Specifications

## Processors

NXP i.MX 8M Plus Family:
- Quad - 4x (or Dual – 2x) Cortex®-A53 cores up to 1.8GHz, Cortex®-M7 core up to 800MHz, Full featured
- Quad - 4x Cortex®-A53 cores up to 1.8GHz, Cortex®-M7 core up to 800MHz, without Neural Processing Unit (NPU)
- Quad Lite - 4x Cortex®-A53 cores up to 1.8GHz, Cortex®-M7 core up to 800MHz, without Hardware Video Codec (VPU), Neural Processing Unit (NPU), and Image Sensor Processor (ISP)

## Memory

Soldered Down LPDDR4-4000 memory, 32-bit interface, up to 6GB

## Graphics

Integrated Graphics Processing Unit GC7000UL
- supports 2 independent displays, OpenGL ES 3.0, Open CL 1.2, Vulkan.
Embedded VPU
- supports H/W decoding of HEVC/H.265, AVC/H.264, VP8, VP9 0.2
- supports H/W ecoding of HEVC/H.265, AVC/H.264

## Video Interfaces

1 x HDMI
1 x LVDS 18/24-bit Single/Dual Channel (factory option)
1 x eDP (factory alternative to one LVDS channel)

## Video Resolution

HDMI, resolution up to 3840x2160 @ 30Hz
LVDS/eDP, resolution up to 1920x1080 @ 60Hz

## Mass Storage

eMMC 5.1 Drive soldered on-board, up to 64GB
SD 1-bit/4-bit SDIO 3.0 interface

## PCI Express

Up to 1 x PCI-e x1 Gen3 port

## Networking

2 x Gigabit Ethernet interface
Optional WiFi 802.11a/b/g/n/ac + BT 5.1 module onboard

## USB

1 x USB 2.0 Host or 1 x USB 2.0 Client port
USB 3.0 Hub onboard, makes available
- 2 x USB 2.0 ports
- 2 x USB 3.0 Superspeed ports

## Audio

Up to 2 x I2S Audio interface (1 x I2S to BLE module as a factory alternative)

## Serial ports

2 x UART Tx/Rx/RTS/CTS
2 x UART Tx/Rx
2 x CAN Bus

## Other Interfaces

1 x 4-lanes (limited bandwidth) + 1 x 2-lanes CSI camera interfaces
I2C Bus
SPI interface
QuadSPI interface
14 x GPI/Os
Boot select signals
Power Management Signals (Standby not supported)

Power supply voltage: +5$V_{DC}$

RTC voltage: 3.3V

Operating temperature:

Commercial version 0°C ÷ +60°C **.
Industrial version –40°C ÷ +85°C **.

Dimensions: 50 x82 mm (1.97" x 3.23")

Supported Operating Systems:

Linux 64-bit

> ! ** Measured at any point of SECO standard heatspreader for this product, during any and all times (including start-up). Actual temperature will widely depend on application, enclosure and/or environment. Upon customer to consider application-specific cooling solutions for the final system to keep the heatspreader temperature in the range indicated.
> Please also check paragraph 4.2

# 2.3 Electrical Specifications

According to SMARC specifications, the SOM-SMARC-MX8M-PLUS module needs to be supplied only with an external +5V$_{DC}$ power supply.

For Real Time Clock working and CMOS memory data retention, it is also needed a backup battery voltage. All these voltages are supplied directly through card edge fingers (see connector's pinout).

All remaining voltages needed for board's working are generated internally from +5V$_{DC}$ power rail.

## 2.3.1 Power Consumption

SOM-SMARC-MX8M-PLUS module, like all SMARC modules, needs a carrier board for its normal working. All connections with the external world come through this carrier board, which also provides the required voltage to the board.

Measurements of power consumption from VDD_IN power rail (5V$_{DC}$) that supplies the board are reported here for 3 different board factory configurations.

| Status | Processor | | |
|---|---|---|---|
| | i.MX 8M Plus Quad 6GB LPDDR4 64GB eMMC | i.MX 8M Plus Quad 4GB LPDDR4 32GB eMMC | i.MX 8M Plus Quad 1GB LPDDR4 4GB eMMC |
| Video | LVDS | HDMI | eDP |
| Idle | 2.78W | 2.59W | 2.23W |
| GPU and CPU working at full load, video reproduction of a 1080p video | 4.87W | 3.95W | 4.52W |
| As above, with active two GbE and two USB 3.0 ports | 6.61W | 5.55W | 5.72W |
| RTC Power consumption on VDD_RTC (when VDD_IN off) | | 300nA | |

Please consider that power consumption is strongly dependent on the board's configuration, on number of processor cores active and from the interfaces that are SW enabled.

## 2.3.2 Power Rails meanings

In all the tables contained in this manual, Power rails are named with the following meaning:

VDD_IN: Module power input voltage. +5V voltage directly coming from the card edge connector.

VDD_RTC: Low current RTC circuit backup power. 3V coin cell voltage coming from the edge card for supplying the RTC clock on the I.MX 8M

_RUN: Switched voltages, i.e. power rails that are active only when the board is in ACPI's S0 (Working) state. Examples: +1.8V_RUN,+3.3V_RUN, +5V_RUN.

_ALW: Always-on voltages, i.e. power rails that are active both in ACPI's S0 (Working), S3 (Standby) and S5 (Soft Off) state. Examples: +5V_ALW, +3.3V_ALW.

## 2.4 Mechanical Specifications

According to SMARC® specifications, the board dimensions are: 50 x 82 mm (1.97" x 3.23") including the pin numbering and edge finger pattern.

Printed circuit of the board is made of ten layers, some of them are ground planes, for disturbance rejection.

The MXM connector accommodates various connector heights for different carrier board applications needs.

When using different connector heights, please consider that, according to SMARC specifications, components placed on bottom side of the module will have a maximum height of 1.3mm. Keep this value in mind when choosing the MXM connector's height, if there is the need to place components on the carrier board in the zone below the SMARC module.
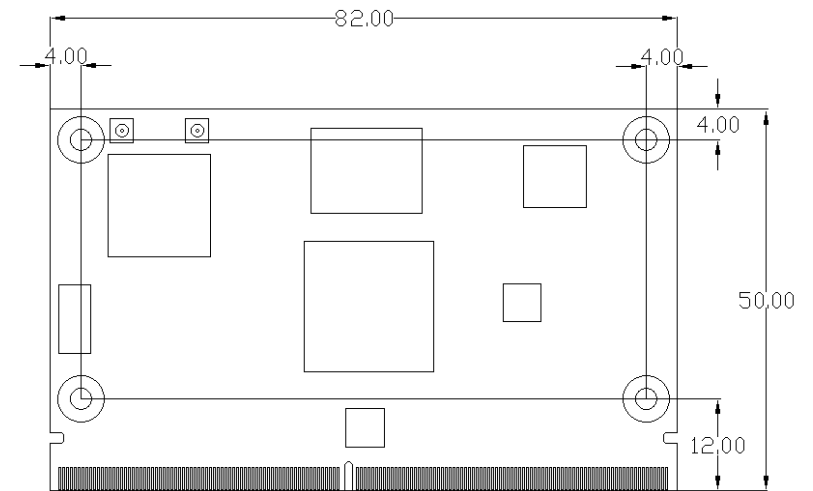


## 2.5 Supported Operating Systems

SOM-SMARC-MX8M-PLUS module supports the following operating systems:

- Linux

SECO will offer the BSP (Board Support Package) for these O.Ss, to reduce at minimum SW development of the board, supplying all the drivers and libraries needed for use both with the SMARC board and the Carrier Board, assuming that the Carrier Board is designed following SECO SMARC Design Guide, with the same IC's.

For further details, please visit https://www.seco.com.

# 2.6 Block Diagram
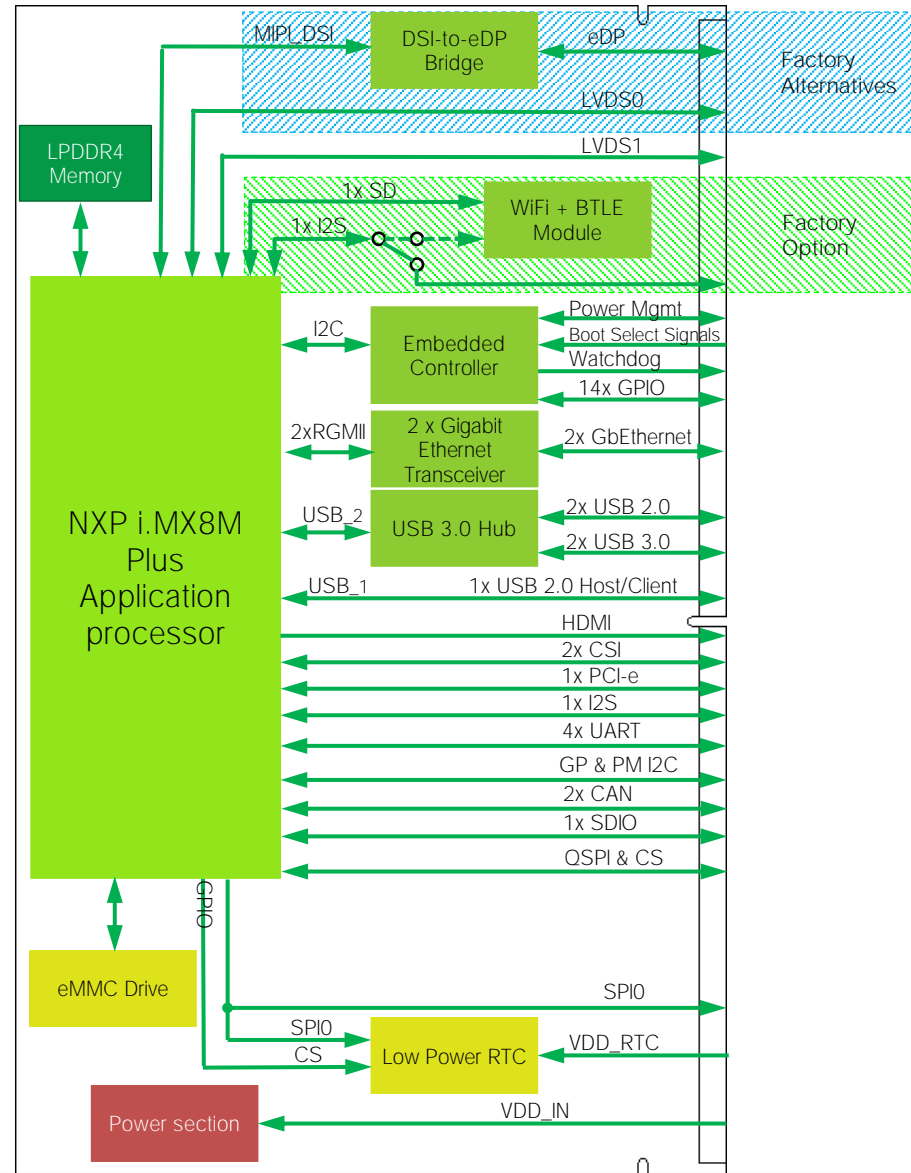
# Chapter 3.
# CONNECTORS

- Introduction
- Connectors description

# 3.1 Introduction

According to SMARC specifications, all interfaces to the board are available through a single card edge connector.

TOP SIDE

BOTTOM SIDE



Card edge golden finger, pin P1

Card edge golden finger, pin P156

Card edge golden finger, pin S158

Card edge golden finger, pin S1

# 3.2 Connectors description

### 3.2.1   WiFi/BTLE Module

This SMARC® module can be equipped, by factory option, with a Dual band (2.4GHz + 5.0 GHz) WLAN 802.11 a/b/g/n/ac + BT 5.0 combo embedded module AzureWave p/n AW-CM276NF.

Aux antenna is used for WLAN and BT while main antenna is used for WLAN only. These are type IPEX MHF4 RF connectors.

### 3.2.2 SMARC® Connector

According to SMARC® Rel 2.1 specification, all interface signals are reported on the card edge connector, which is a 314-pin Card Edge that can be inserted into standard low profile 314 pin 0.5mm right pitch angle connector that was originally defined for use with MXM3 graphics cards.

Not all signals contemplated in the SMARC® Rel 2.1 are implemented on card edge connector, therefore, please refer to the following table for a list of effective signals reported on the card edge connector.

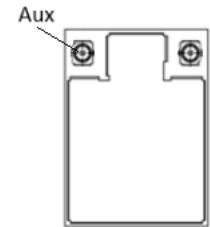Consider that the signals labelled as RSVD are for factory production use only and shall be left unused, otherwise the module may not boot or function properly.

For accurate signals description, please consult the following paragraphs.

| SMARC® Golden Finger Connector – CN2 | | | | | | | |
|---|---|---|---|---|---|---|---|
| TOP SIDE | | | | BOTTOM SIDE | | | |
| SIGNAL GROUP | Type | Pin name | Pin nr. | Pin nr. | Pin name | Type | SIGNAL GROUP |
|  |  |  |  | S1 | I2C_CAM1_CK | O | CAMERA |
| MANAGEMENT | I | SMB_ALERT_1V8# | P1 | S2 | I2C_CAM1_DAT | I/O | CAMERA |
|  |  | GND | P2 | S3 | GND |  |  |
| CAMERA | I | CSI1_CK+ | P3 | S4 | RSVD |  |  |
| CAMERA | I | CSI1_CK- | P4 | S5 | I2C_CAM0_CK | O | CAMERA |
| GBE | I/O | GBE1_SDP | P5 | S6 | CAM_MCK | O | CAMERA |
| GBE | I/O | GBE0_SDP | P6 | S7 | I2C_CAM0_DAT | I/O | CAMERA |
| CAMERA | I | CSI1_RX0+ | P7 | S8 | CSI0_CK+ | I | CAMERA |
| CAMERA | I | CSI1_RX0- | P8 | S9 | CSI0_CK- | I | CAMERA |
|  |  | GND | P9 | S10 | GND |  |  |
| CAMERA | I | CSI1_RX1+ | P10 | S11 | CSI0_RX0+ | I | CAMERA |
| CAMERA | I | CSI1_RX1- | P11 | S12 | CSI0_RX0- | I | CAMERA |
|  |  | GND | P12 | S13 | GND |  |  |
| CAMERA | I | CSI1_RX2+ | P13 | S14 | CSI0_RX1+ | I | CAMERA |
| CAMERA | I | CSI1_RX2- | P14 | S15 | CSI0_RX1- | I | CAMERA |
|  |  | GND | P15 | S16 | GND |  |  |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| CAMERA | I | CSI1_RX3+ | P16 | S17 | GBE1_MDI0+ | I/O | GBE |
| CAMERA | I | CSI1_RX3- | P17 | S18 | GBE1_MDI0- | I/O | GBE |
| | | GND | P18 | S19 | GBE1_LINK100# | O | GBE |
| GBE | I/O | GBE0_MDI3- | P19 | S20 | GBE1_MDI1+ | I/O | GBE |
| GBE | I/O | GBE0_MDI3+ | P20 | S21 | GBE1_MDI1- | I/O | GBE |
| GBE | O | GBE0_LINK100# | P21 | S22 | GBE1_LINK1000# | O | GBE |
| GBE | O | GBE0_LINK1000# | P22 | S23 | GBE1_MDI2+ | I/O | GBE |
| GBE | I/O | GBE0_MDI2- | P23 | S24 | GBE1_MDI2- | I/O | GBE |
| GBE | I/O | GBE0_MDI2+ | P24 | S25 | GND | | |
| GBE | O | GBE0_LINK_ACT# | P25 | S26 | GBE1_MDI3+ | I/O | GBE |
| GBE | I/O | GBE0_MDI1- | P26 | S27 | GBE1_MDI3- | I/O | GBE |
| GBE | I/O | GBE0_MDI1+ | P27 | S28 | N.C. | | |
| | | N.C. | P28 | S29 | N.C. | | |
| GBE | I/O | GBE0_MDI0- | P29 | S30 | N.C. | | |
| GBE | I/O | GBE0_MDI0+ | P30 | S31 | GBE1_LINK_ACT# | O | GBE |
| SPI_INTERFACE | O | SPI0_CS1# | P31 | S32 | N.C. | | |
| | | GND | P32 | S33 | N.C. | | |
| SDIO_CARD | I | SDIO_WP | P33 | S34 | GND | | |
| SDIO_CARD | I/O | SDIO_CMD | P34 | S35 | USB4+ | I/O | USB |
| SDIO_CARD | I | SDIO_CD# | P35 | S36 | USB4- | I/O | USB |
| SDIO_CARD | O | SDIO_CK | P36 | S37 | N.C. | | |
| SDIO_CARD | O | SDIO_PWR_EN | P37 | S38 | AUDIO_MCK | O | AUDIO |
| | | GND | P38 | S39 | I2S0_LRCK | I/O | AUDIO |
| SDIO_CARD | I/O | SDIO_D0 | P39 | S40 | I2S0_SDOUT | O | AUDIO |
| SDIO_CARD | I/O | SDIO_D1 | P40 | S41 | I2S0_SDIN | I | AUDIO |
| SDIO_CARD | I/O | SDIO_D2 | P41 | S42 | I2S0_CK | O | AUDIO |
| SDIO_CARD | I/O | SDIO_D3 | P42 | S43 | N.C. | | |
| SPI_INTERFACE | O | SPI0_CS0# | P43 | S44 | N.C. | | |
| SPI_INTERFACE | O | SPI0_CK | P44 | S45 | N.C. | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| SPI_INTERFACE | I | SPI0_DIN | P45 | S46 | N.C. | | |
| SPI_INTERFACE | O | SPI0_DO | P46 | S47 | GND | | |
| | | GND | P47 | S48 | I2C_GP_CK | I/O | I2C |
| | | N.C. | P48 | S49 | I2C_GP_DAT | I/O | I2C |
| | | N.C. | P49 | S50 | I2S2_LRCK | I/O | AUDIO |
| | | GND | P50 | S51 | I2S2_SDOUT | O | AUDIO |
| | | N.C. | P51 | S52 | I2S2_SDIN | I | AUDIO |
| | | N.C. | P52 | S53 | I2S2_CK | O | AUDIO |
| | | GND | P53 | S54 | N.C. | | |
| SPI_INTERFACE | O | QSPI_CS0# | P54 | S55 | USB5_EN_OC# | I/O | USB |
| SPI_INTERFACE | O | QSPI_CS1# | P55 | S56 | QSPI_IO_2 | I/O | SPI_INTERFACE |
| SPI_INTERFACE | O | QSPI_CK | P56 | S57 | QSPI_IO_3 | I/O | SPI_INTERFACE |
| SPI_INTERFACE | I/O | QSPI_IO_1 | P57 | S58 | N.C. | | |
| SPI_INTERFACE | I/O | QSPI_IO_0 | P58 | S59 | N.C. | | |
| | | GND | P59 | S60 | N.C. | | |
| USB | I/O | USB0+ | P60 | S61 | GND | | |
| USB | I/O | USB0- | P61 | S62 | USB3_SSTX+ | O | USB |
| USB | I/O | USB0_EN_OC# | P62 | S63 | USB3_SSTX- | O | USB |
| USB | I | USB0_VBUS_DET | P63 | S64 | GND | | |
| USB | I | USB0_OTG_ID | P64 | S65 | USB3_SSRX+ | I | USB |
| USB | I/O | USB1+ | P65 | S66 | USB3_SSRX- | I | USB |
| USB | I/O | USB1- | P66 | S67 | GND | | |
| USB | I/O | USB1_EN_OC# | P67 | S68 | USB3+ | I/O | USB |
| | | GND | P68 | S69 | USB3- | I/O | USB |
| USB | I/O | USB2+ | P69 | S70 | GND | | |
| USB | I/O | USB2- | P70 | S71 | USB2_SSTX+ | O | USB |
| USB | I/O | USB2_EN_OC# | P71 | S72 | USB2_SSTX- | O | USB |
| | | RESERVED | P72 | S73 | GND | | |
| | | N.C | P73 | S74 | USB2_SSRX+ | I | USB |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| USB | I/O | USB3_EN_OC# | P74 | S75 | USB2_SSRX- | I | USB |
| PCI_e | O | PCIE_A_RST# | P75 | S76 | N.C. | | |
| USB | I/O | USB4_EN_OC# | P76 | S77 | N.C. | | |
| PCI_e | I/O | PCIE_B_CKREQ# | P77 | S78 | N.C. | | |
| PCI_e | I/O | PCIE_A_CKREQ# | P78 | S79 | N.C. | | |
| | | GND | P79 | S80 | GND | | |
| | | N.C. | P80 | S81 | N.C. | | |
| | | N.C. | P81 | S82 | N.C. | | |
| | | GND | P82 | S83 | GND | | |
| PCI_e | O | PCIE_A_REFCK+ | P83 | S84 | N.C. | | |
| PCI_e | O | PCIE_A_REFCK- | P84 | S85 | N.C. | | |
| | | GND | P85 | S86 | GND | | |
| PCI_e | I | PCIE_A_RX+ | P86 | S87 | N.C. | | |
| PCI_e | I | PCIE_A_RX- | P87 | S88 | N.C. | | |
| | | GND | P88 | S89 | GND | | |
| PCI_e | O | PCIE_A_TX+ | P89 | S90 | N.C. | | |
| PCI_e | O | PCIE_A_TX- | P90 | S91 | N.C. | | |
| | | GND | P91 | S92 | GND | | |
| SECONDARY_DISPLAY | O | HDMI_D2+ | P92 | S93 | N.C. | | |
| SECONDARY_DISPLAY | O | HDMI_D2- | P93 | S94 | N.C. | | |
| | | GND | P94 | S95 | N.C. | | |
| SECONDARY_DISPLAY | O | HDMI_D1+ | P95 | S96 | N.C. | | |
| SECONDARY_DISPLAY | O | HDMI_D1- | P96 | S97 | N.C. | | |
| | | GND | P97 | S98 | N.C. | | |
| SECONDARY_DISPLAY | O | HDMI_D0+ | P98 | S99 | N.C. | | |
| SECONDARY_DISPLAY | O | HDMI_D0- | P99 | S100 | N.C. | | |
| | | GND | P100 | S101 | GND | | |
| SECONDARY_DISPLAY | O | HDMI_CK+ | P101 | S102 | N.C. | | |
| SECONDARY_DISPLAY | O | HDMI_CK- | P102 | S103 | N.C. | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | GND | P103 | S104 | N.C. | | |
| SECONDARY_DISPLAY | I | HDMI_HPD | P104 | S105 | N.C. | | |
| SECONDARY_DISPLAY | I/O | HDMI_CTRL_CK | P105 | S106 | N.C. | | |
| SECONDARY_DISPLAY | I/O | HDMI_CTRL_DAT | P106 | S107 | LCD1_BKLT_EN | O | LCD_SUPPORT |
| | | N.C. | P107 | S108 | LVDS1_CK+ | O | PRIMARY_DISPLAY |
| GPIO | I/O | GPIO0 / CAM0_PWR# | P108 | S109 | LVDS1_CK- | O | PRIMARY_DISPLAY |
| GPIO | I/O | GPIO1 / CAM1_PWR# | P109 | S110 | GND | | |
| GPIO | I/O | GPIO2 / CAM0_RST# | P110 | S111 | LVDS1_0+ | O | PRIMARY_DISPLAY |
| GPIO | I/O | GPIO3 / CAM1_RST# | P111 | S112 | LVDS1_0- | O | PRIMARY_DISPLAY |
| GPIO | I/O | GPIO4 / HDA_RST# | P112 | S113 | N.C. | | |
| GPIO | I/O | GPIO5 / PWM_OUT | P113 | S114 | LVDS1_1+ | O | PRIMARY_DISPLAY |
| GPIO | I/O | GPIO6 / TACHIN | P114 | S115 | LVDS1_1- | O | PRIMARY_DISPLAY |
| GPIO | I/O | GPIO7 | P115 | S116 | LCD1_VDD_EN | O | LCD_SUPPORT |
| GPIO | I/O | GPIO8 | P116 | S117 | LVDS1_2+ | O | PRIMARY_DISPLAY |
| GPIO | I/O | GPIO9 | P117 | S118 | LVDS1_2- | O | PRIMARY_DISPLAY |
| GPIO | I/O | GPIO10 | P118 | S119 | GND | | |
| GPIO | I/O | GPIO11 | P119 | S120 | LVDS1_3+ | O | PRIMARY_DISPLAY |
| | | GND | P120 | S121 | LVDS1_3- | O | PRIMARY_DISPLAY |
| MANAGEMENT | I/O | I2C_PM_CK | P121 | S122 | LCD1_BKLT_PWM | O | LCD_SUPPORT |
| MANAGEMENT | I/O | I2C_PM_DAT | P122 | S123 | GPIO13 | I/O | GPIO |
| BOOT_SEL | I | BOOT_SEL0# | P123 | S124 | GND | | |
| BOOT_SEL | I | BOOT_SEL1# | P124 | S125 | LVDS0_0+ / eDP0_TX0+ | O | PRIMARY_DISPLAY |
| BOOT_SEL | I | BOOT_SEL2# | P125 | S126 | LVDS0_0- / eDP0_TX0- | O | PRIMARY_DISPLAY |
| MANAGEMENT | O | RESET_OUT# | P126 | S127 | LCD0_BKLT_EN | O | LCD_SUPPORT |
| MANAGEMENT | I | RESET_IN# | P127 | S128 | LVDS0_1+ / eDP0_TX1+ | O | PRIMARY_DISPLAY |
| MANAGEMENT | I | POWER_BTN# | P128 | S129 | LVDS0_1- / eDP0_TX1+ | O | PRIMARY_DISPLAY |
| ASYNC_SERIAL | O | SER0_TX | P129 | S130 | GND | | |
| ASYNC_SERIAL | I | SER0_RX | P130 | S131 | LVDS0_2+ / eDP0_TX2+ | O | PRIMARY_DISPLAY |
| ASYNC_SERIAL | O | SER0_RTS# | P131 | S132 | LVDS0_2- / eDP0_TX2- | O | PRIMARY_DISPLAY |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ASYNC_SERIAL | I | SER0_CTS# | P132 | S133 | LCD0_VDD_EN | O | LCD_SUPPORT |
| | | GND | P133 | S134 | LVDS0_CK+ / eDP0_AUX+ | O | PRIMARY_DISPLAY |
| ASYNC_SERIAL | O | SER1_TX | P134 | S135 | LVDS0_CK- / eDP0_AUX+ | O | PRIMARY_DISPLAY |
| ASYNC_SERIAL | I | SER1_RX | P135 | S136 | GND | | |
| ASYNC_SERIAL | O | SER2_TX | P136 | S137 | LVDS0_3+ / eDP0_TX3+ | O | PRIMARY_DISPLAY |
| ASYNC_SERIAL | I | SER2_RX | P137 | S138 | LVDS0_3- / eDP0_TX3+ | O | PRIMARY_DISPLAY |
| ASYNC_SERIAL | O | SER2_RTS# | P138 | S139 | I2C_LCD_CK | O | LCD_SUPPORT |
| ASYNC_SERIAL | I | SER2_CTS# | P139 | S140 | I2C_LCD_DAT | I/O | LCD_SUPPORT |
| ASYNC_SERIAL | O | SER3_TX | P140 | S141 | LCD0_BKLT_PWM | O | LCD_SUPPORT |
| ASYNC_SERIAL | I | SER3_RX | P141 | S142 | GPIO12 | I/O | GPIO |
| | | GND | P142 | S143 | GND | | |
| CAN | O | CAN0_TX | P143 | S144 | eDP0_HPD | I | PRIMARY_DISPLAY |
| CAN | I | CAN0_RX | P144 | S145 | WDT_TIME_OUT# | O | WATCHDOG |
| CAN | O | CAN1_TX | P145 | S146 | PCIE_WAKE# | I | PCI_e |
| CAN | I | CAN1_RX | P146 | S147 | VDD_RTC | | |
| | | VDD_IN | P147 | S148 | LID# | I | MANAGEMENT |
| | | VDD_IN | P148 | S149 | SLEEP# | I | MANAGEMENT |
| | | VDD_IN | P149 | S150 | VIN_PWR_BAD# | I | MANAGEMENT |
| | | VDD_IN | P150 | S151 | CHARGING# | I | MANAGEMENT |
| | | VDD_IN | P151 | S152 | CHARGER_PRSNT# | I | MANAGEMENT |
| | | VDD_IN | P152 | S153 | CARRIER_STBY# | O | MANAGEMENT |
| | | VDD_IN | P153 | S154 | CARRIER_PWR_ON | O | MANAGEMENT |
| | | VDD_IN | P154 | S155 | FORCE_RECOV# | I | BOOT_SEL |
| | | VDD_IN | P155 | S156 | BATLOW# | I | MANAGEMENT |
| | | VDD_IN | P156 | S157 | TEST# | I | MANAGEMENT |
| | | | | S158 | GND | | |

### 3.2.2.1 LCD Display Support Signals

The panel control signals are:

LCD0_VDD_EN: Panel #0 VDD enable signal. Set high to enable. +1.8V_RUN electrical level Output.

LCD0_BKLT_EN: Panel #0 Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_RUN electrical level Output

LCD0_BKLT_PWM: This signal can be used to adjust the Panel #0 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_RUN electrical level Output

LCD1_VDD_EN: Panel #1 VDD enable signal. Set high to enable. +1.8V_RUN electrical level Output

LCD1_BKLT_EN: Panel #1 Backlight Enable signal. It can be used to turn On/Off the backlight's lamps of a connected LVDS display. +1.8V_RUN electrical level Output.

LCD1_BKLT_PWM: This signal can be used to adjust the Panel #1 backlight brightness in displays supporting Pulse Width Modulated (PWM) regulations. +1.8V_RUN electrical level Output.

I2C LCD signals are managed by SoC I2C2 bus.

I2C_LCD_DAT: LCD I2C Data. This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level Bidirectional with a 2k2Ω pull-up resistor.

I2C_LCD_CLK: LCD I2C Clock: This signal is used to read the LCD display EDID EEPROM. +1.8V_RUN electrical level Output with a 2k2Ω pull-up resistor.

On this bus a selection of addresses must be left reserved for on-board peripherals as presented in this table (also consider that this bus is shared with CAM0 from par. 3.2.2.4):

| I2C2 Bus | |
|---|---|
| Address | Peripheral |
| 0x2D | DSI Bridge |
| 0x25 | USB Hub |

Please refer to the following schematics as an example of connection of LCD display control signals and supply voltage selection jumpers.
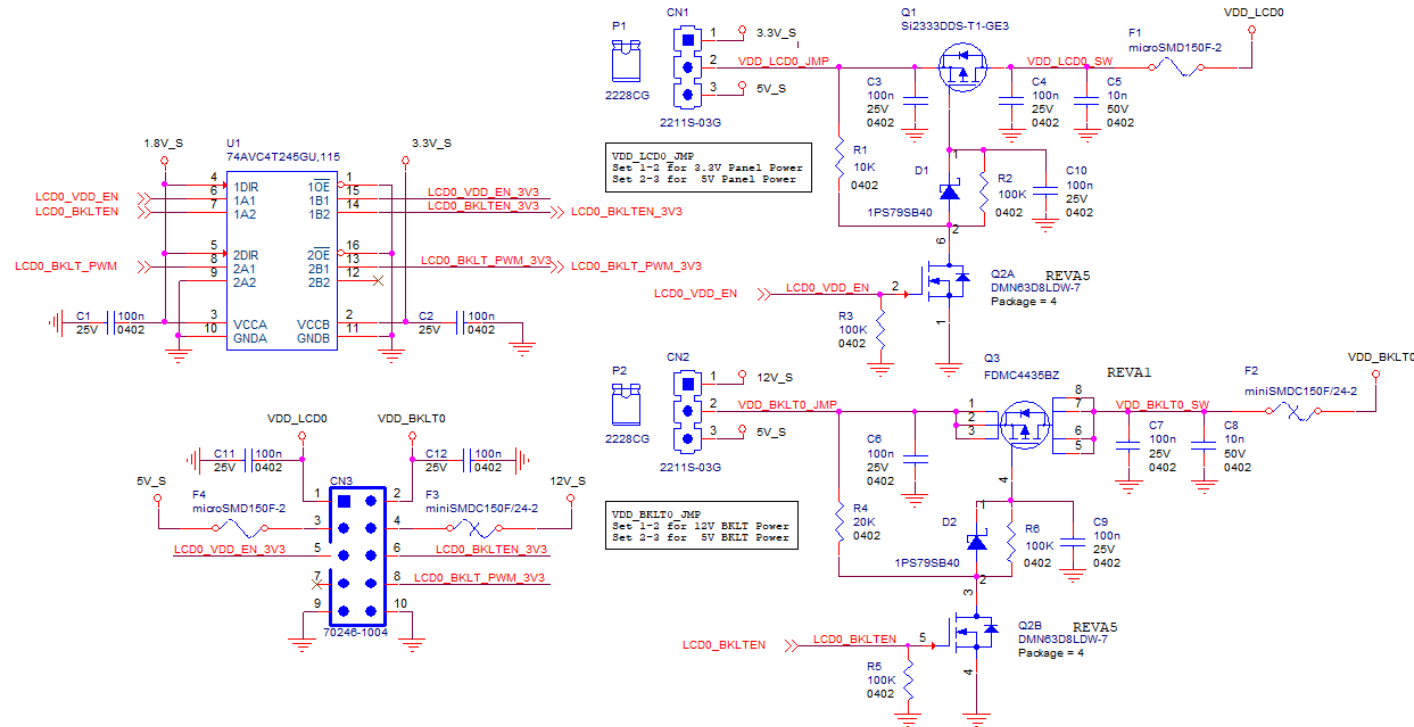


### 3.2.2.2 eDP / Dual Channel LVDS (factory alternatives)

A dual channel LVDS interface is natively supported by the SOC, with a maximum supported resolution of 1920x1200 @ 60Hz, while an eDP interface can be selected as a factory alternative to be present on the edge pinout in place of Channel #0 of the LVDS interface.

ONLY ONE set of signals from the following two sets are present, dependent on the factory board configuration.

EITHER the signals for Channel #0 are LVDS:

LVDS0_0+/LVDS0_0-: LVDS Channel #0 differential data pair #0.

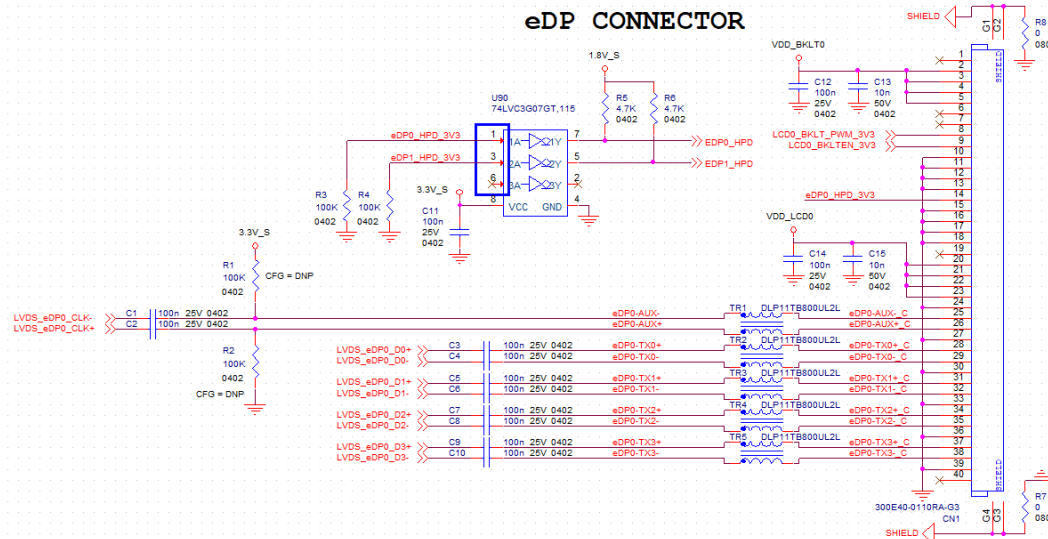LVDS0_1+/LVDS0_1-: LVDS Channel #0 differential data pair #1.

LVDS0_2+/LVDS0_2-: LVDS Channel #0 differential data pair #2.

LVDS0_3+/LVDS0_3-: LVDS Channel #0 differential data pair #3.

LVDS0_CK+/LVDS0_CK-: LVDS Channel #0 differential Clock.

OR the signals for Channel #0 are eDP:

eDP0_TX0+/ eDP0_TX0-: eDP Channel #0 differential data pair #0.

eDP0_TX1+/ eDP0_TX1-: eDP Channel #0 differential data pair #1.

eDP0_TX2+/ eDP0_TX2-: eDP Channel #0 differential data pair #2.

eDP0_TX3+/ eDP0_TX3-: eDP Channel #0 differential data pair #3.

eDP0_AUX+/ eDP0_AUX-: eDP Channel #0 differential Clock.

eDP0_HPD: Hot Plug Detect, Active high Input signal of +1.8V_RUN electrical level from carrier board. 1MΩ pull-down resistor is placed on module for this signal.

Please refer to the following schematics as an example of connection of eDP interface on the carrier board. Hot Plug Detect signal must be buffered to



prevent back feeding of power from the display to the module as well as level translation.

The signals for Channel #1 of the LVDS interface is always available on the edge pinout regardless of the factory board configuration.

LVDS1_1+ / LVDS1_0- : LVDS Channel #1 differential data pair #0

LVDS1_1+/ LVDS1_1-: LVDS Channel #1 differential data pair #1

LVDS1_2+/LVDS1_2-: LVDS Channel #1 differential data pair #2

LVDS1_3+/ LVDS1_3-: LVDS Channel #1 differential data pair #3

LVDS1_CK+/ LVDS1_CK-: LVDS Channel #1 differential Clock

Please refer to the following schematics as an example of connection of dual channel LVDS interface on the carrier board, with EMI filtering section included.



LVDS CONNECTORS
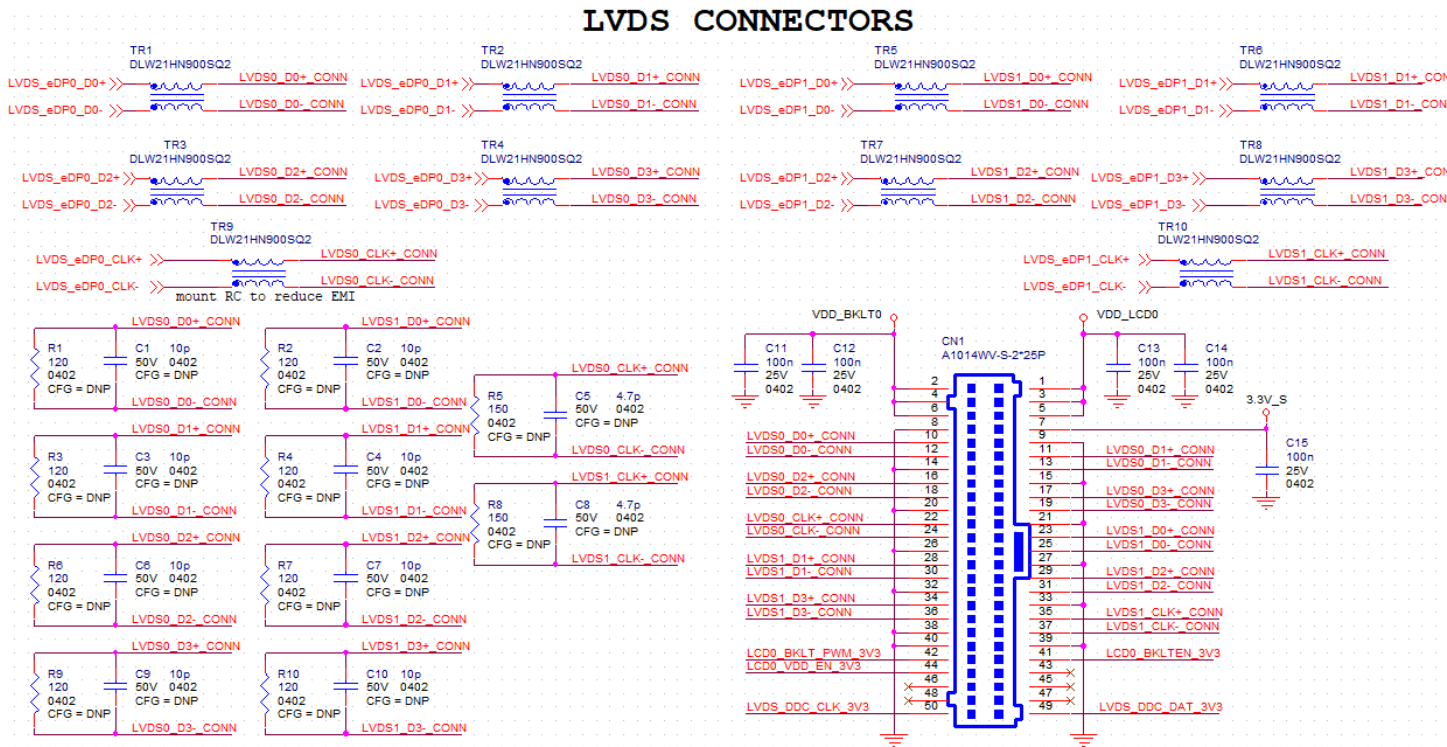
### 3.2.2.3   Secondary Display (HDMI interface) signals

The NXP i.MX 8M processor has an HD Display Transmitter Controller (HDMI TX), which provides a HDMI interface with resolution limited by the NXP SoC up to 3840x2160 @ 30Hz.

The signals are:

HDMI_D0+/HDMI_D0-: HDMI Output Differential Pair #0

HDMI_D1+/HDMI_D1-: HDMI Output Differential Pair #1

HDMI_D2+/HDMI_D2-: HDMI Output Differential Pair #2

HDMI_CK+/HDMI_CK-: HDMI Differential Clock

HDMI_HPD: Hot Plug Detect Input signal. +1.8V_RUN electrical level signal

HDMI_CTRL_CK: DDC Clock line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

HDMI_CTRL_DAT: DDC Data line for HDMI panel. Bidirectional signal, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

Since HDMI Tx module is embedded in the i.MX 8M processors it is not necessary to implement voltage level shifter for TMDS differential pairs on the Carrier board. It is still necessary, however, to implement voltage level shifters on Control data/Clock signals, as well as for Hot Plug Detect signal.

### 3.2.2.4   Serial Cameras

There are two MIPI-CSI2 interfaces available. The CSI0 interface supports two lanes, the CSI1 interface supports 4 lanes with limited bandwidth. Consider that from the SoC the CSI0 interface is managed by the MIPI_CSI1 group signals and I2C2 bus, while CSI1 is managed by MIPI_CSI2 group signals and I2C3 bus.

CSI0_CK+/CSI0_CK-: 2-lane CSI Input Clock Differential Pair

CSI0_RX0+/CSI0_RX0-: 2-lane CSI Input Differential Pair 0

CSI0_RX1+/CSI0_RX1-: 2-lane CSI Input Differential Pair 1

CSI1_CK+/CSI1_CK-: 4-lane CSI Input Clock Differential Pair

CSI1_RX0+/CSI1_RX0- 4-lane CSI Input Differential Pair 0

CSI1_RX1+/CSI1_RX1-: 4-lane CSI Input Differential Pair 1

CSI1_RX2+/CSI1_RX2-: 4-lane CSI Input Differential Pair 2

CSI1_RX3+/CSI1_RX3-: 4-lane CSI Input Differential Pair 3

CAM_MCK: Master clock Output for CSI Port #0 and/or #1 support, electrical level 1.8V_RUN

I2C_CAM0_CK: CSI Port #0 dedicated I2C Bus Clock signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

I2C_CAM0_DAT: CSI Port #0 dedicated I2C Bus Data signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

On this bus a selection of addresses must be left reserved for on-board peripherals as presented in this table (also consider that this bus is shared with LCD signals from par. 3.2.2.1):

| I2C2 Bus | |
|---|---|
| Address | Peripheral |
| 0x2D | DSI Bridge |
| 0x25 | USB Hub |

I2C_CAM1_CK: CSI Port #1 dedicated I2C Bus Clock signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

I2C_CAM1_DAT: CSI Port #1 dedicated I2C Bus Data signal, Bi-Directional, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor.

On this bus a selection of addresses must be left reserved for on-board peripherals as presented in this table:

| I2C3 Bus | |
|---|---|
| Address | Peripheral |
| 0x68 | PCIe Clock Generator |
| 0x20 | I/O Expander |

### 3.2.2.5   SDI/O interface signals

The NXP i.MX 8M Plus processors offer many different SDIO interfaces, that can be used independently one from the other to implement different mass storages (internal eMMC, internal SD Card, external SDI/O interface).

The SDIO3 signals of the processor are used for the onboard eMMC storage of the module.

The SDIO1 signals of the processor are used for the factory optional onboard WiFi/BTLE module.

The SDIO2 interface of the processor is externally accessible through the edge connector of the module. Supporting 4-bit mode as per the SMARC specification.

The uSDHC controller complies with:

- SD Host Controller Standard Specification version 3.0 with SDR104 signaling to support up to 104MB/sec.

- MMC System Specification version 5.0

The edge accessible SDIO2 signals are as follows:

SDIO_WP: Write Protect bidirectional signal, electrical level +1.8V_RUN (SDR104) or +3.3V_RUN with 10kΩ pull-up resistor. It is used to communicate the status of Write Protect switch on external SD/MMC card.

SDIO_CMD: Command/Response line. Used to send command from Host (i.MX 8M processor) to the connected card, and to send the response from the card to the Host.

SDIO_CD#: Card Detect Input. Active Low Signal, electrical level +1.8V_RUN (SDR104) or +3.3V_RUN with 10kΩ pull-up resistor. This signal must be externally pulled low to signal that a SDIO/MMC Card is present.

SDIO_CK: Clock Line (output), up to 200MHz maximum frequency for SDR104 Mode (4-bit only).

SDIO_PWR_EN: SDIO Power Enable output, active high signal, electrical level +1.8V_RUN (SDR104) or +3.3V_RUN with 2.2kΩ pull-up resistor. It is used to enable the power line supplying SD/SDIO/MMC devices.

SDIO_[D0÷D3]: SDIO data bus. Signals for 4-bit SD/SDIO/MMC communication mode.

Please refer to the following schematics as an example of connection of SDIO interface on the carrier board, with Voltage clamping diodes highly recommended on all signal lines for ESD suppression.
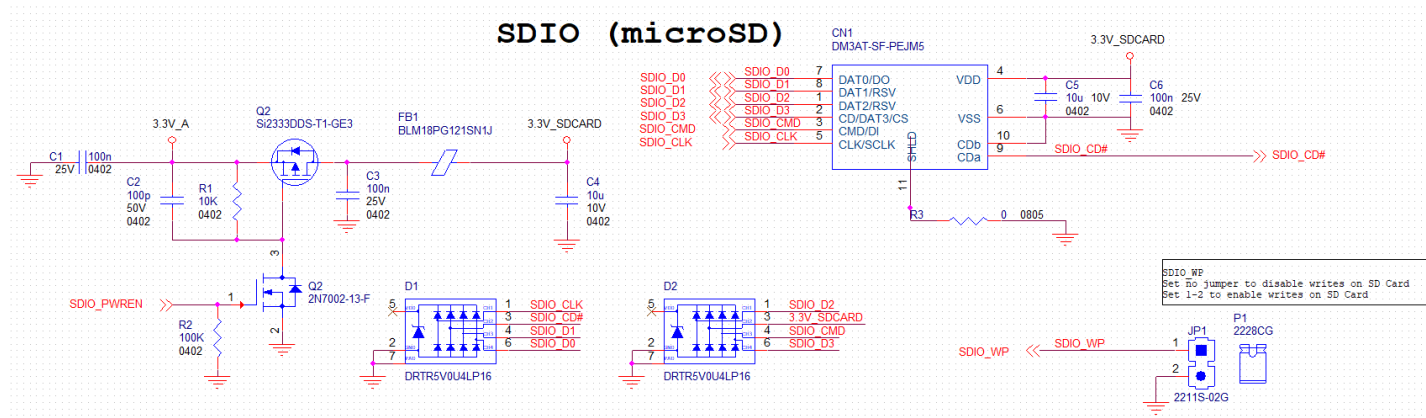
### 3.2.2.6 SPI interface signals

The signals related to SPI0 are as follows:

SPI0_CS0#: SPI primary Chip select, active low output signal. Electrical level +1.8V_RUN

SPI0_CS1#: SPI secondary Chip select, active low output signal. Electrical level +1.8V_RUN. This signal must be used only in case there are two SPI devices on the carrier board, and the first chip select signal (SPI_CS0#) has already been used. It must not be used in case there is only one SPI device

SPI0_CK: SPI Clock Output to carrier board's SPI embedded devices. Electrical level +1.8V_RUN

SPI0_DIN: SPI0 Master Data Input, electrical level +1.8V_RUN. Input to i.MX 8M from SPI devices embedded on the Carrier Board.

SPI0_DO: SPI0 Master Data Output, electrical level +1.8V_RUN. Output from i.MX 8M to SPI devices embedded on the Carrier Board

The signals related to QuadSPI are as follows:

QSPI_CS0#: QuadSPI primary Chip select, active low output signal. Electrical level +1.8V_RUN.

QSPI_CS1#: QuadSPI secondary Chip select, active low output signal. Electrical level +1.8V_RUN.

QSPI_CK: QuadSPI Master Clock Output. Electrical level +1.8V_RUN. The reference timing signal for all the serial input and output operations

QSPI_IO_[0:3]: QuadSPI Master Data Bidirectional . Electrical level +1.8V_RUN. Data transfer between the master and slaves. In Single I/O mode, QSPI_IO_0 is the QSPI master output/QSPI slave input (MOSI) whereas QSPI_IO_1 is the QSPI master input/QSPI slave output (MISO).

SPI interface can support speed up to 20MHz.

### 3.2.2.7 Audio interface signals

Here are following the signals related to I2S Audio interfaces:

The first I2S interface managed by the SAI2 group of signals of the SoC is always available on the edge pinout:

AUDIO_MCK: Master clock output to Audio codec. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_LRCK: Left& Right audio synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDOUT: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_SDIN: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN

I2S0_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

A second I2S interface managed by the SAI3 group of signals of the SoC is available by default on the edge pinout; as a factory alternative can be routed to the BTLE module to support Bluetooth Audio.

I2S2_LRCK: Left& Right audio synchronization clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

I2S2_SDOUT: Digital audio Output. Output from the module to the Carrier board, electrical level +1.8V_RUN

I2S2_SDIN: Digital audio Input. Input from the module to the Carrier board, electrical level +1.8V_RUN

I2S2_CK: Digital audio clock. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN

Signals routed to the Carrier Board have to be connected to I2S Audio Codecs. Please refer to the chosen Codec's Reference Design Guide for correct implementation of audio section on the carrier board.

### 3.2.2.8   I2C Interface

I2C General Purpose signals are managed by SoC I2C5 bus.

I2C_GP_CK: I2C General Purpose clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor

I2C_GP_DAT: I2C General Purpose data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_RUN with a 2k2Ω pull-up resistor

On this bus a selection of addresses must be left reserved for on-board peripherals as presented in this table:

| I2C5 Bus | |
|----------|-----------|
| Address | Peripheral |
| 0x50 | EEPROM |

I2C Power Management signals are managed by SoC I2C1 bus.

I2C_PM_CK: Power management clock signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_ALW with 2.2kΩ pull-up resistor.

I2C_PM_DAT: Power management data signal. Bi-Directional between the module to the Carrier board, electrical level +1.8V_ALW with 2.2kΩ pull-up resistor

On this bus a selection of addresses must be left reserved for on-board peripherals as presented in this table:

| I2C1 Bus | |
|----------|-----------|
| Address | Peripheral |
| 0x40 | Embedded Controller |
| 0x25 | PMIC |
| 0x48 | Secure Element |

### 3.2.2.9 Asynchronous Serial Ports (UART) interface signals

All UART interface signals are directly managed by the i.MX 8M Plus processor. In all versions, the edge connector offers the four following UART interfaces.

SER0_TX: UART #2 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

SER0_RX: UART #2 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER0_RTS#: UART #2 Interface, Handshake signal, Request to Send (output) line, +1.8V_RUN electrical level

SER0_CTS#: UART #2 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER1_TX: UART #4 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

SER1_RX: UART #4 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER2_TX: UART #3 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

SER2_RX: UART #3 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER2_RTS#: UART #3 Interface, Handshake signal, Request to Send (output) line, +1.8V_RUN electrical level

SER2_CTS#: UART #3 Interface, Handshake signal, Clear to Send (Input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor.

SER3_RX: UART #1 Interface, Serial data Receive (input) line, +1.8V_RUN electrical level with a 100kΩ pull-up resistor

SER3_TX: UART #1 Interface, Serial data Transmit (output) line, +1.8V_RUN electrical level

Please consider that interface is at +1.8V_RUN electrical level; therefore, please evaluate well the typical scenario of application. If there isn't any explicit need of interfacing directly at +1.8V_RUN level, for connection to standard serial ports commonly available (like those offered by common PCs, for example) it is mandatory to include an RS-232 transceiver on the carrier board.

In the following schematic here is an example of UART interface on the carrier board, with a multiprotocol transceiver allowing to support RS485/RS-422/RS-232 serial interfaces.



## SER #0
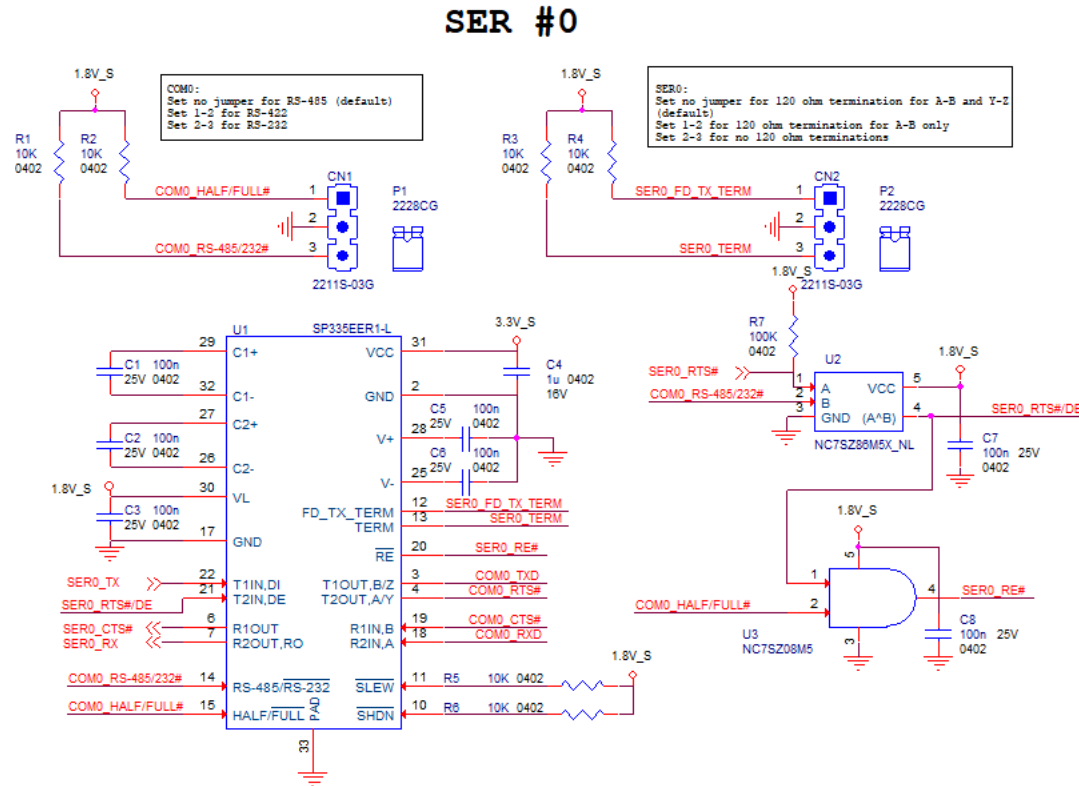
### 3.2.2.10  USB interface signals

The module has 5x USB ports consisting of 1x USB 2.0 port from the NXP i.MX 8M Plus processor USB 2.0 controller which can be configured at kernel compile time to work as Host or Client, 2x USB 3.0 Superspeed and 2x USB 2.0 from a Cypress USB3304-68LTXC USB 3.0 hub controller.

Here following the signals related to USB interfaces.

USB0+/ USB0-: Universal Serial Bus 2.0 Port #0 differential pair (directly managed by i.MX 8M USB Host Controller core #1).

USB0_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for over current operation information.
The USB0 port is directly managed by i.MX 8M Plus USB Host Controller core #1 and can be used for serial download driving FORCE_RECOV# low.
Please take note that the OTG functionality on this port is not supported at runtime, USB0 must be set to work as Client or Host at kernel compile time.

USB1+/ USB1-: Universal Serial Bus Port 2.0 #1 differential pair.

USB1_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for OC operation information.

USB2+/USB2-: Universal Serial Bus Port 2.0 #2 differential pair.

USB2_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for OC operation information.

USB3+/USB3-: Universal Serial Bus Port 2.0 #3 differential pair.

USB3_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for OC operation information.

USB4+/USB4-: Universal Serial Bus Port 2.0 #4 differential pair.

USB4_EN_OC#: Power Enable and over current monitoring function. Active Low Output signal, +3.3V_ALW electrical level with a 10kΩ pull-up resistor. Refer to SMARC® 2.1 Specification for OC operation information.

USB5_EN_OC#: not managed. Tied to GND through a 10kΩ pull-down resistor

USB2_SSTX+/ USB2_SSTX-: USB 3.0 Port #1 Superspeed Transmit differential pair.

USB2_SSRX+/ USB2_SSRX-: USB 3.0 Port #1 Superspeed Receive differential pair.

USB3_SSTX+/ USB3_SSTX-: USB 3.0 Port #2 Superspeed Transmit differential pair.

USB3_SSRX+/ USB3_SSRX-: USB 3.0 Port #2 Superspeed Receive differential pair.

For EMI/ESD protection, common mode chokes on USB data lines, and clamping diodes on USB data and voltage lines, are also needed. Switch with settable current limit on power lines are recommended.
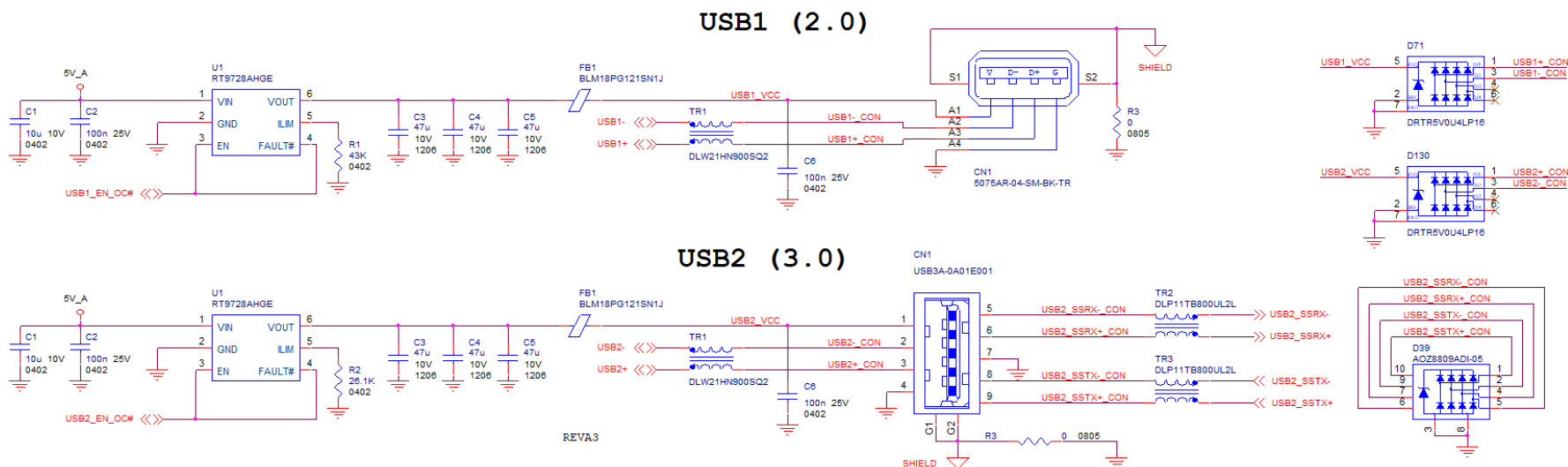


### 3.2.2.11 PCI Express interface signals

The module can offer one PCI Express x1 lanes, which is directly managed by i.MX 8M Plus processor (PCI express Gen 3.0 is supported).

Here following the signals involved in PCI express management

PCIE_A_RX+/ PCIE_A_RX-: PCI Express lane #0, Transmitting Output Differential pair

PCIE_A_TX+/PCIE_A_TX-: PCI Express lane #0, Receiving Input Differential pair

PCIE_A_REFCK+/ PCIE_A_REFCK-: PCI Express Reference Clock for lane #0, Differential Pair

PCIE_A_RST#: Reset Signal that is sent from SMARC® Module to a PCI-e device available on the carrier board. Active Low, +3.3V_RUN electrical level.

PCIE_A_CKREQ#: PCIe Port A clock request, can be used for power saving mode on PCIe. Active low, driven by open drain circuitry on the carrier board.

PCIE_WAKE#: PCIe wake up interrupt to host input signal. Active low, +3.3V_ALW electrical level.

### 3.2.2.12 Gigabit Ethernet signals

Gigabit Ethernet interfaces are realized on the module using two Texas Instruments DP83867CRRGZR Gigabit Ethernet transceivers, which are interfaced to NXP i.MX 8M Plus processor through RGMII interface.

Here following the signals involved in Gigabit Ethernet #0 management:

GBE0_MDI0+/GBE0_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair

GBE0_MDI1+/GBE0_MDI1-: Media Dependent Interface (MDI) Transmit differential pair

GBE0_MDI2+/GBE0_MDI2-: Media Dependent Interface (MDI) Transmit differential pair

GBE0_MDI3+/GBE0_MDI3-: Media Dependent Interface (MDI) Transmit differential pair

GBE0_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE0_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE0_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE0_SDP: Software defined pin, directly managed by TI Gigabit Ethernet PHY transceiver #0. Bidirectional signal, +3.3V_ALW electrical level.

Here following the signals involved in Gigabit Ethernet #1 management:

GBE1_MDI0+/GBE1_MDI0-: Media Dependent Interface (MDI) Transmit/Receive differential pair

GBE1_MDI1+/GBE1_MDI1-: Media Dependent Interface (MDI) Transmit differential pair

GBE1_MDI2+/GBE1_MDI2-: Media Dependent Interface (MDI) Transmit differential pair

GBE1_MDI3+/GBE1_MDI3-: Media Dependent Interface (MDI) Transmit differential pair

GBE1_LINK_ACT#: Ethernet controller activity indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE1_LINK100#: Ethernet controller 100Mbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE1_LINK1000#: Ethernet controller 1Gbps link indicator. Active Low Output signal, +3.3V_ALW electrical level

GBE1_SDP: Software defined pin, directly managed by TI Gigabit Ethernet PHY transceiver #1. Bidirectional signal, +3.3V_ALW electrical level.

Please refer to the following schematics as an example of connection of Ethernet interface on the carrier board, with TVS diodes specifically designed to protect sensitive components which are connected to high-speed data and transmission lines from overvoltage caused by ESD. In this example, it is also present GBE_CTREF signal connected on pin #2 of the RJ-45 connector. TI Gigabit Ethernet PHY transceiver, however, doesn't need the analog powered centre tap, therefore the signal GBE_CTREF is not available on SMARC® connector.

Please notice that if just a FastEthernet (i.e. 10/100 Mbps) is needed, then only MDI0 and MDI1 differential lanes are necessary, for both Gigabit Ethernet interfaces
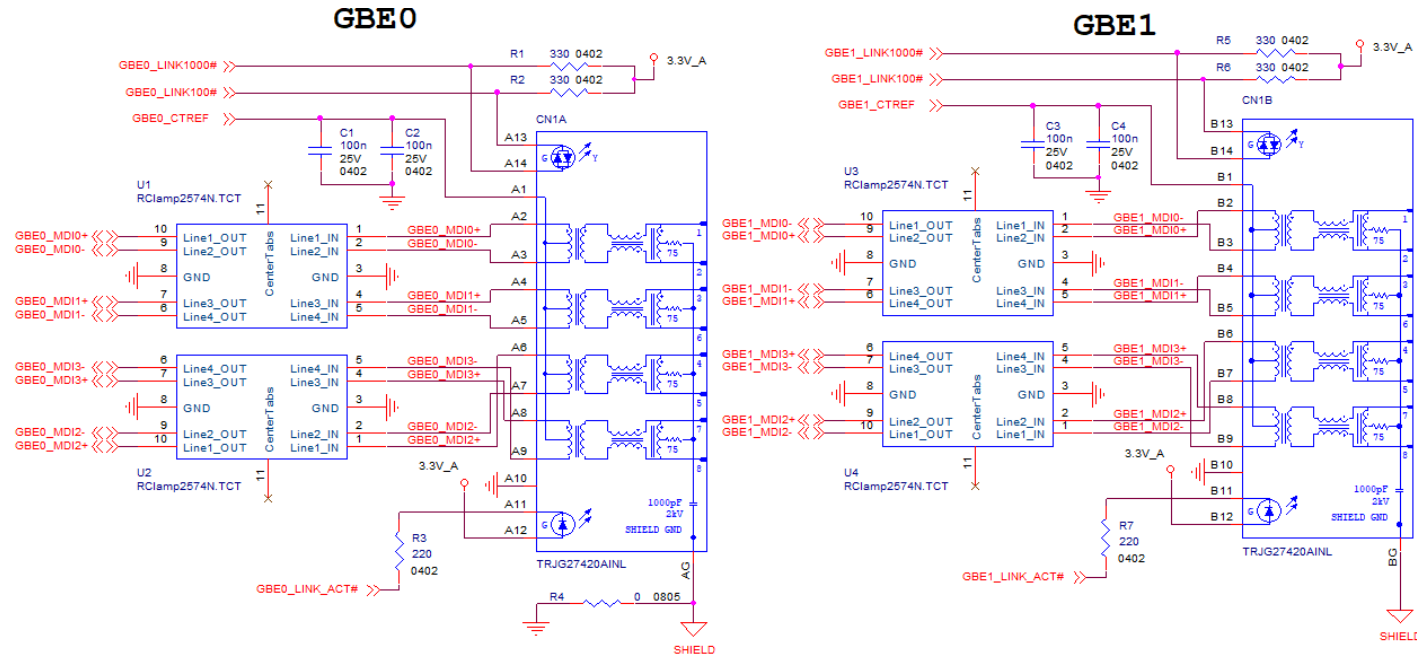


### 3.2.2.13 CAN interface signals

Two available CAN interfaces signals are directly managed by the i.MX 8M Plus processor.

CAN0_TX: CAN Transmit Output for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal with a 2k2Ω pull-up resistor

CAN0_RX: CAN Receive Input for CAN Bus Channel 0. +1.8V_RUN electrical voltage level signal with a 2k2Ω pull-up resistor

CAN1_TX: CAN Transmit Output for CAN Bus Channel 1. +1.8V_RUN electrical voltage level signal with a 2k2Ω pull-up resistor

CAN1_RX: CAN Receive Input for CAN Bus Channel 1. +1.8V_RUN electrical voltage level signal with a 2k2Ω pull-up resistor

Please consider that it is not possible to connect the SMARC® CAN interface to any CAN Bus directly, it is necessary to integrate a CAN Bus Transceiver in the Carrier board.

### 3.2.2.14 Watchdog

WDT_TIME_OUT#: Watchdog timer Output. +1.8V_RUN electrical level

### 3.2.2.15 Miscellaneous signals

GPIO0 / CAM0_PWR#: General Purpose I/O #0, +1.8V_RUN electrical level

GPIO1 / CAM1_PWR#: General Purpose I/O #1, +1.8V_RUN electrical level

GPIO2 / CAM0_RST#: General Purpose I/O #2, +1.8V_RUN electrical level

GPIO3 / CAM1_RST#: General Purpose I/O #3, +1.8V_RUN electrical level

GPIO4 / HDA_RST#: General Purpose I/O #4, +1.8V_RUN electrical level

GPIO5 / PWM_OUT: General Purpose I/O #5, +1.8V_RUN electrical level

GPIO6 / TACHIN: General Purpose I/O #6, +1.8V_RUN electrical level

GPIO7: General Purpose I/O #7, +1.8V_RUN electrical level

GPIO8: General Purpose I/O #8, +1.8V_RUN electrical level

GPIO9: General Purpose I/O #9, +1.8V_RUN electrical level

GPIO10: General Purpose I/O #10, +1.8V_RUN electrical level

GPIO11: General Purpose I/O #11, +1.8V_RUN electrical level

GPIO12: General Purpose I/O #12, +1.8V_RUN electrical level

GPIO13: General Purpose I/O #13, +1.8V_RUN electrical level

### 3.2.2.16 Management pins

According to the SMARC® specifications, the input pins listed below are all Active Low, meant to be driven by open drain devices on the carrier board:

VIN_PWR_BAD#: Power Bad indication signal from the Carrier Board

CARRIER_PWR_ON: Power On. Command to the Carrier Board. Output, +1.8V_ALW electrical level

CARRIER_STBY#: Stand By command to the Carrier Board. Output, +1.8V_ALW electrical level

RESET_OUT#: General Purpose Reset. Output, +1.8V_ALW electrical level

RESET_IN#: General Purpose Reset. Input, +3.3V_ALW electrical level

POWER_BTN#: Power Button. Input, +3.3V_ALW electrical level

SLEEP#: Sleep indicator from Carrier board. Input, +3.3V_ALW electrical level (Standby not supported)

LID#: LID Switch. Input, +3.3V_ALW electrical level

BATLOW#: Battery Low indication signal from the Carrier Board. Input, +3.3V_ALW electrical level

CHARGING#: Battery Charging Input Signal from the Carrier Board. Input, +3.3V_ALW electrical level

CHARGER_PRSNT#: Battery Charger Present input from the Carrier Board. Input, +3.3V_ALW electrical level

TEST#: Held low by Carrier to invoke Module vendor specific test function(s). Input. +3.3V_ALW electrical level with a 10kΩ pull-up resistor

SMB_ALERT_1V8#: SM Bus Alert# (interrupt) signal. Input, +1.8V_ALW electrical level with a 2k2Ω pull-up resistor

### 3.2.2.17 Boot Select

The following signals are active low and driven by open drain circuitry on the carrier board.

BOOT_SEL0#: Boot Device Selection #0. Input, +1.8V_ALW electrical level with a 10kΩ pull-up resistor

BOOT_SEL1#: Boot Device Selection #1. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor

BOOT_SEL2#: Boot Device Selection #2. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor

FORCE_RECOV#: Force recovery Mode. Input, +1.8V_ ALW electrical level with a 10kΩ pull-up resistor

# Chapter 4.
## Appendices

- Thermal Design

# 4.1 SoC to Connector Pinout

Some of the signals available on the SMARC® Edge Connector can be reprogrammed to implement different functionalities, according to the i.MX 8M pin-multiplexing possibilities.

In this table is presented the list of connector signals which are connected to the SoC with the corresponding SoC pad and name. Consult the i.MX 8M documentation for the multiplexing capabilities of the listed pads.

| SMARC® Golden Finger Connector – CN2 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| TOP SIDE | | | | | BOTTOM SIDE | | | |
| SoC signal | SoC pad | Pin name | Pin nr. | Pin nr. | Pin name | SoC pad | SoC signal | |
| | | | | S1 | I2C_CAM1_CK | AJ7 | I2C3_SCL | |
| | | | P1 | S2 | I2C_CAM1_DAT | AJ6 | I2C3_SDA | |
| | | | P2 | S3 | | | | |
| MIPI_CSI2_CLK_P | A23I | CSI1_CK+ | P3 | S4 | | | | |
| MIPI_CSI2_CLK_N | B23 | CSI1_CK- | P4 | S5 | I2C_CAM0_CK | AH6 | I2C2_SCL | |
| | | | P5 | S6 | CAM_MCK | A4 | GPIO1_IO14 | |
| | | | P6 | S7 | I2C_CAM0_DAT | AE8 | I2C2_SDA | |
| MIPI_CSI2_D0_P | A25 | CSI1_RX0+ | P7 | S8 | CSI0_CK+ | D22 | MIPI_CSI1_CLK_P | |
| MIPI_CSI2_D0_N | B25 | CSI1_RX0- | P8 | S9 | CSI0_CK- | E22 | MIPI_CSI1_CLK_N | |
| | | | P9 | S10 | | | | |
| MIPI_CSI2_D1_P | A24 | CSI1_RX1+ | P10 | S11 | CSI0_RX0+ | D18 | MIPI_CSI1_D0_P | |
| MIPI_CSI2_D1_N | B24 | CSI1_RX1- | P11 | S12 | CSI0_RX0- | E18 | MIPI_CSI1_D0_N | |
| | | | P12 | S13 | | | | |
| MIPI_CSI2_D2_P | A22 | CSI1_RX2+ | P13 | S14 | CSI0_RX1+ | D20 | MIPI_CSI1_D1_P | |
| MIPI_CSI2_D2_N | B22 | CSI1_RX2- | P14 | S15 | CSI0_RX1- | E20 | MIPI_CSI1_D1_N | |
| | | | P15 | S16 | | | | |
| MIPI_CSI2_D3_P | A21 | CSI1_RX3+ | P16 | S17 | | | | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| MIPI_CSI2_D3_N | B21 | CSI1_RX3- | P17 | S18 | | | |
| | | | P18 | S19 | | | |
| | | | P19 | S20 | | | |
| | | | P20 | S21 | | | |
| | | | P21 | S22 | | | |
| | | | P22 | S23 | | | |
| | | | P23 | S24 | | | |
| | | | P24 | S25 | | | |
| | | | P25 | S26 | | | |
| | | | P26 | S27 | | | |
| | | | P27 | S28 | | | |
| | | | P28 | S29 | | | |
| | | | P29 | S30 | | | |
| | | | P30 | S31 | | | |
| SAI5_RXC | AD14 | SPI0_CS1# | P31 | S32 | | | |
| | | | P32 | S33 | | | |
| SD2_WP | AC26 | SDIO_WP | P33 | S34 | | | |
| SD2_CMD | AB28 | SDIO_CMD | P34 | S35 | | | |
| SD2_CD_B | AD29 | SDIO_CD# | P35 | S36 | | | |
| SD2_CLK | AB29 | SDIO_CK | P36 | S37 | | | |
| SD2_RESET_B | AD28 | SDIO_PWR_EN | P37 | S38 | AUDIO_MCK | AJ15 | SAI2_MCLK |
| | | | P38 | S39 | I2S0_LRCK | AJ17 | SAI2_TXFS |
| SD2_DATA0 | AC28 | SDIO_D0 | P39 | S40 | I2S0_SDOUT | AH16 | SAI2_TXD0 |
| SD2_DATA1 | AC29 | SDIO_D1 | P40 | S41 | I2S0_SDIN | AJ14 | SAI2_RXD0 |
| SD2_DATA2 | AA26 | SDIO_D2 | P41 | S42 | I2S0_CK | AH15 | SAI2_TXC |
| SD2_DATA3 | AA25 | SDIO_D3 | P42 | S43 | | | |
| ECSPI2_SS0 | AJ22 | SPI0_CS0# | P43 | S44 | | | |
| ECSPI2_SCLK | AH21 | SPI0_CK | P44 | S45 | | | |
| ECSPI2_MISO | AH20 | SPI0_DIN | P45 | S46 | | | |

| Signal | Pin | Alt | # | # | Signal | Pin | Alt |
|---|---|---|---|---|---|---|---|
| ECSPI2_MOSI | AJ21 | SPI0_DO | P46 | S47 | | | |
| | | | P47 | S48 | I2C_GP_CK | AE18 | SPDIF_TX |
| | | | P48 | S49 | I2C_GP_DAT | AD18 | SPDIF_RX |
| | | | P49 | S50 | I2S2_LRCK | AC16 | SAI3_TXFS |
| | | | P50 | S51 | I2S2_SDOUT | AH18 | SAI3_TXD |
| | | | P51 | S52 | I2S2_SDIN | AF18 | SAI3_RXD |
| | | | P52 | S53 | I2S2_CK | AH19 | SAI3_TXC |
| | | | P53 | S54 | | | |
| NAND_CE0_B | L26 | QSPI_CS0# | P54 | S55 | | | |
| NAND_READY_B | T28 | QSPI_CS1# | P55 | S56 | QSPI_IO_2 | L24 | NAND_DATA02 |
| NAND_ALE | N25 | QSPI_CK | P56 | S57 | QSPI_IO_3 | N24 | NAND_DATA03 |
| NAND_DATA01 | L25 | QSPI_IO_1 | P57 | S58 | | | |
| NAND_DATA00 | R25 | QSPI_IO_0 | P58 | S59 | | | |
| | | | P59 | S60 | | | |
| USB1_D_P | D10 | USB0+ | P60 | S61 | | | |
| USB1_D_N | E10 | USB0- | P61 | S62 | | | |
| SAI1_TXD7 / GPIO1_IO12 | AJ13 / A5 | USB0_EN_OC# | P62 | S63 | | | |
| USB1_VBUS | A11 | USB0_VBUS_DET | P63 | S64 | | | |
| GPIO1_IO10 | B7 | USB0_OTG_ID | P64 | S65 | | | |
| | | | P65 | S66 | | | |
| | | | P66 | S67 | | | |
| | | | P67 | S68 | | | |
| | | | P68 | S69 | | | |
| | | | P69 | S70 | | | |
| | | | P70 | S71 | | | |
| | | | P71 | S72 | | | |
| | | | P72 | S73 | | | |
| | | | P73 | S74 | | | |
| | | | P74 | S75 | | | |

| | | | | |
|---|---|---|---|---|
| SD1_DATA5 | AA29 | PCIE_A_RST# | P75 | S76 |
| | | | P76 | S77 |
| 3V3_RUN / SWDIO | N.A. | PCIE_B_CKREQ# | P77 | S78 |
| 2C4_SCL | AF8 | PCIE_A_CKREQ# | P78 | S79 |
| | | | P79 | S80 |
| | | | P80 | S81 |
| | | | P81 | S82 |
| | | | P82 | S83 |
| | | | P83 | S84 |
| | | | P84 | S85 |
| | | | P85 | S86 |
| PCIE_RXN_P | A14 | PCIE_A_RX+ | P86 | S87 |
| PCIE_RXN_N | B14 | PCIE_A_RX- | P87 | S88 |
| | | | P88 | S89 |
| PCIE_TXN_P | A15 | PCIE_A_TX+ | P89 | S90 |
| PCIE_TXN_N | B15 | PCIE_A_TX- | P90 | S91 |
| | | | P91 | S92 |
| HDMI_TX2_P | AH27 | HDMI_D2+ | P92 | S93 |
| HDMI_TX2_N | AJ27 | HDMI_D2- | P93 | S94 |
| | | | P94 | S95 |
| HDMI_TX1_P | AH26 | HDMI_D1+ | P95 | S96 |
| HDMI_TX1_N | AJ26 | HDMI_D1- | P96 | S97 |
| | | | P97 | S98 |
| HDMI_TX0_P | AH25 | HDMI_D0+ | P98 | S99 |
| HDMI_TX0_N | AJ25 | HDMI_D0- | P99 | S100 |
| | | | P100 | S101 |
| HDMI_TXC_P | AH24 | HDMI_CK+ | P101 | S102 |
| HDMI_TXC_N | AJ24 | HDMI_CK- | P102 | S103 |
| | | | P103 | S104 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| HDMI_HPD | AE22 | HDMI_HPD | P104 | S105 | | | | |
| HDMI_DDC_SCL | AC22 | HDMI_CTRL_CK | P105 | S106 | | | | |
| HDMI_DDC_SDA | AF22 | HDMI_CTRL_DAT | P106 | S107 | | | | |
| | | | P107 | S108 | LVDS1_CK+ | A28 | LVDS1_CLK_P | |
| | | | P108 | S109 | LVDS1_CK- | B28 | LVDS1_CLK_N | |
| | | | P109 | S110 | | | | |
| | | | P110 | S111 | LVDS1_0+ | A26 | LVDS1_D0_P | |
| | | | P111 | S112 | LVDS1_0- | B26 | LVDS1_D0_N | |
| | | | P112 | S113 | | | | |
| GPIO1_IO11 | D8 | GPIO5 / PWM_OUT | P113 | S114 | LVDS1_1+ | A27 | LVDS1_D1_P | |
| | | | P114 | S115 | LVDS1_1- | B27 | LVDS1_D1_N | |
| | | | P115 | S116 | | | | |
| SAI2_RXC | AJ16 | GPIO8 | P116 | S117 | LVDS1_2+ | B29 | LVDS1_D2_P | |
| SAI3_RXFS | AJ19 | GPIO9 | P117 | S118 | LVDS1_2- | C28 | LVDS1_D2_N | |
| SAI1_RXC | AH8 | GPIO10 | P118 | S119 | | | | |
| SAI1_RXFS | AJ9 | GPIO11 | P119 | S120 | LVDS1_3+ | C29 | LVDS1_D3_P | |
| | | | P120 | S121 | LVDS1_3- | D28 | LVDS1_D3_N | |
| I2C1_SCL | AC8 | I2C_PM_CK | P121 | S122 | LCD1_BKLT_PWM | AJ20 | SAI3_MCLK | |
| I2C1_SDA | AH7 | I2C_PM_DAT | P122 | S123 | GPIO13 | B8 | GPIO1_IO09 | |
| | | | P123 | S124 | | | | |
| | | | P124 | S125 | LVDS0_0+ / eDP0_TX0+ | D29 / N.A. | LVDS0_D0_P / N.A. | |
| | | | P125 | S126 | LVDS0_0- / eDP0_TX0- | E28 / N.A. | LVDS0_D0_N / N.A. | |
| | | | P126 | S127 | LCD0_BKLT_EN | A3 | GPIO1_IO06 | |
| | | | P127 | S128 | LVDS0_1+ / eDP0_TX1+ | E29 / N.A. | LVDS0_D1_P / N.A. | |
| | | | P128 | S129 | LVDS0_1- / eDP0_TX1+ | F28 / N.A. | LVDS0_D1_N / N.A. | |
| UART2_TXD | AH4 | SER0_TX | P129 | S130 | | | | |
| UART2_RXD | AF6 | SER0_RX | P130 | S131 | LVDS0_2+ / eDP0_TX2+ | G29 / N.A. | LVDS0_D2_P / N.A. | |
| SAI3_RXC | AJ18 | SER0_RTS# | P131 | S132 | LVDS0_2- / eDP0_TX2+ | H28 / N.A. | LVDS0_D2_N / N.A. | |
| SD1_DATA4 | U26 | SER0_CTS# | P132 | S133 | LCD0_VDD_EN | AH17 | SAI2_RXFS | |

| | | | P133 | S134 | LVDS0_CK+ /eDP0_AUX+ | F29 / N.A. | LVDS0_CLK_P / N.A. |
|---|---|---|---|---|---|---|---|
| UART4_TXD | AH5 | SER1_TX | P134 | S135 | LVDS0_CK- / eDP0_AUX+ | G28 / N.A. | LVDS0_CLK_N / N.A. |
| UART4_RXD | AF5 | SER1_RX | P135 | S136 | | | |
| ECSPI1_MOSI | AC20 | SER2_TX | P136 | S137 | LVDS0_3+ / eDP0_TX3+ | H29 / N.A. | LVDS0_D3_P / N.A. |
| ECSPI1_SCLK | AF20 | SER2_RX | P137 | S138 | LVDS0_3- / eDP0_TX3+ | J28 / N.A. | LVDS0_D3_N / N.A. |
| ECSPI1_MISO | AD20 | SER2_RTS# | P138 | S139 | I2C_LCD_CK | AH6 | I2C2_SCL |
| ECSPI1_SS0 | AE20 | SER2_CTS# | P139 | S140 | I2C_LCD_DAT | AE8 | I2C2_SDA |
| UART1_TXD | AJ3 | SER3_TX | P140 | S141 | LCD0_BKLT_PWM | AC18 | SPDIF_EXT_CLK |
| UART1_RXD | AD6 | SER3_RX | P141 | S142 | GPIO12 | A8 | GPIO1_IO08 |
| | | | P142 | S143 | | | |
| SAI5_RXD1 | AD16 | CAN0_TX | P143 | S144 | | | |
| SAI5_RXD2 | AF16 | CAN0_RX | P144 | S145 | | | |
| SAI5_RXD3 | AE14 | CAN1_TX | P145 | S146 | | | |
| SAI5_MCLK | AF14 | CAN1_RX | P146 | S147 | | | |
| | | | | S148 | | | |
| | | | | S149 | | | |
| | | | | S150 | | | |
| | | | | S151 | | | |
| | | | | S152 | | | |
| | | | | S153 | | | |
| | | | | S154 | | | |
| | | | | S155 | | | |
| | | | | S156 | | | |
| | | | | S157 | | | |
| | | | | S158 | | | |

## 4.2 Thermal Design

Highly integrated modules like SOM-SMARC-MX8M-PLUS offer very high performance within small dimensions. On the other hand, the miniaturization of ICs and the high operating frequencies of the processors lead to high heat generation that must be dissipated in order to maintain the CPU within its allowed temperature range.

The operating temperature specified in the Technical Features of SOM-SMARC-MX8M-PLUS module indicates the temperature range in which any and all parts of the heat spreader / heat sink must remain, in order for SECO to guarantee functionality. Hence, these numbers do not necessarily indicate the suitable environmental temperature.

The heat spreader is not intended to be a guaranteed standalone cooling system, but should be used only as a supplemental means of transferring heat to another dissipation system (i.e. heat sinks, fans, heat pipes etc).

It is the customer's responsibility to design and apply an application-dependent cooling system, capable of ensuring that the heat spreader / heat sink temperature remain within the indicated range of the module.

It is an absolute requirement that the customer, after thorough evaluation of the processor's workload in the actual system application, the system enclosure and consequent air flow/Thermal analysis, accurately study and develop a suitable cooling solution for the assembled system.

SECO can provide SOM-SMARC-MX8M-PLUS module specific heatspreaders and heatsinks, but please remember that their use must be evaluated accurately inside the final system, and that they should be used only as a part of a more comprehensive ad-hoc cooling solutions.

| Ordering Code | Description |
|---|---|
| RD18-DISS-1-PK | SMARC® HEAT SPREADER: SOM-SMARC-MX8M-PLUS Heat Spreader (PASSIVE) - Packaged |
| RD18-DISS-2-PK | SMARC® HEAT SINK: SOM-SMARC-MX8M-PLUS Heat Sink (PASSIVE) - Packaged |

⚠️ **Warning!**

The thermal solutions available with SECO boards are tested in the commercial temperature range (0-60°C), without housing and inside climatic chamber. Therefore, the customer is suggested to study, develop and validate the cooling solution for his system, considering ambient temperature, processor's workload, utilisation scenarios, enclosures, air flow and so on.

In particular, the heatspreader is not intended to be a cooling system by itself, but only as the standard means for transferring heat to cooler, like heatsinks, cold plate, heat pipes and so on.

**SECO**

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